HTR Main FPGA

PCB: Rev4.3

Complete documentation on http://cmsdoc.cern.ch/cms/HCAL/document/CountingHouse/HTR/

Last changes in blue color

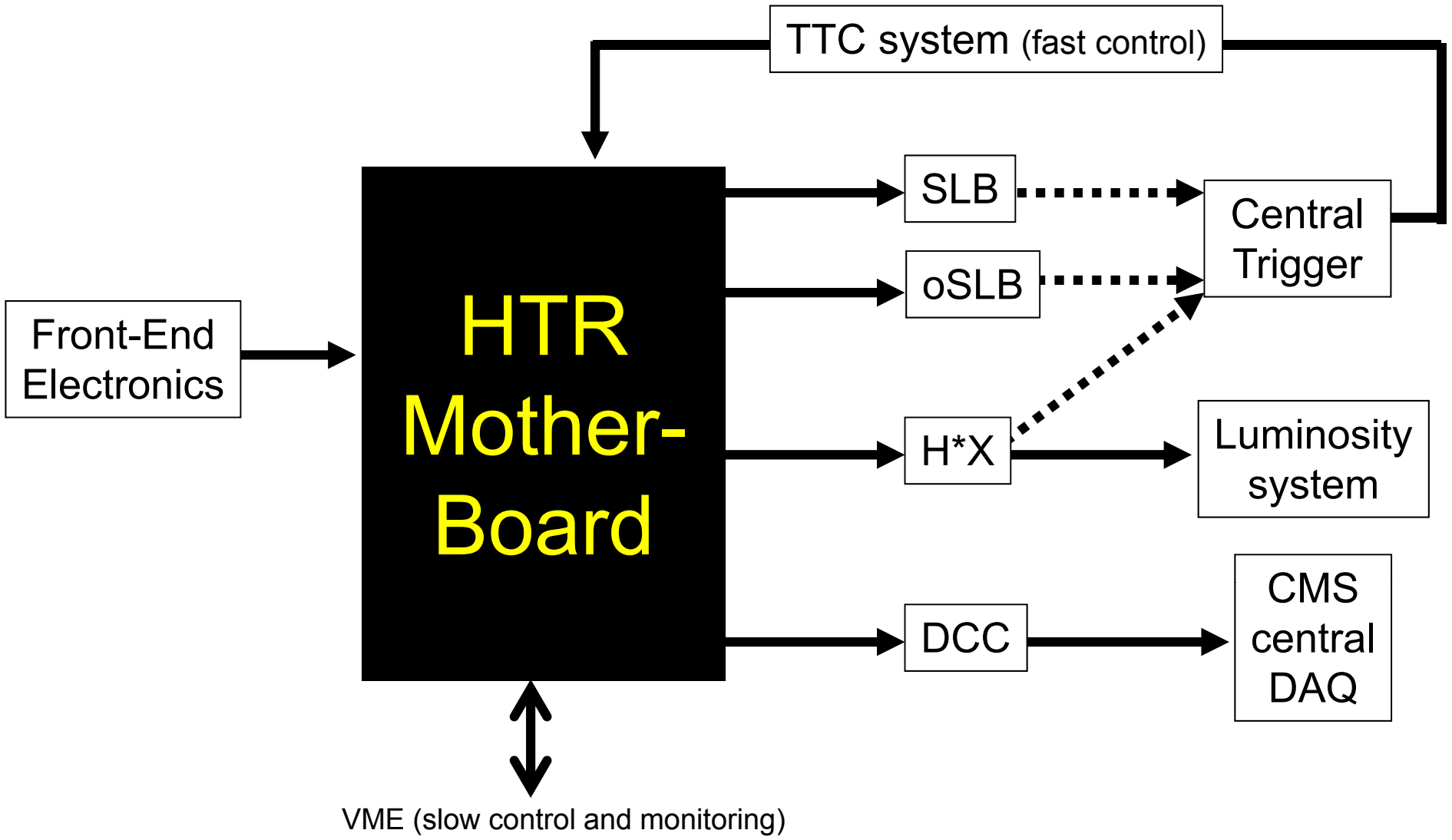
FEATURES in NORMAL BEAM MODE

- One HTR board includes two almost identical logic sub-modules (Top and Bottom). The only logical difference is the TTCreset signal, connected to Top FPGA only. Top and bottom FPGAs accept the same firmware
- Over 17 firmware variations ("flavors") support different trigger and luminosity outputs
- Fast control over TTC; slow control and monitoring over VME
- Each sub-module (1 FPGA + other stuff) receives 8 fibers x (8b/10b) x 1.6Gb/s data (as from HCAL FE-cards)
- Detect FE Orbit Message (Normal message only) and IDLE-to-DATA transitions of the 8 input fibers (in order to monitor time-alignment).
- Generate Trigger Primitives with a latency ~15 clock ticks (40 MHz clock) for the whole FPGA
- Trigger must arrive less than 6us after data (adjustable latency)
- Detect triggers violating TDR rule 1 [No more than 1 trigger per 3 BXs] and 2 [No more than 2 triggers per 25 BXs]
- When triggered, acquire a programmable number of QIE data-samples = NumSamples and of Trigger Primitives = NumSamplesT.
- Requirements: NumSamples must be an even number, with 2 ≤ NumSamples ≤ 20; ; if NumSamples < 11 then NumSamplesT must be 0 ≤ NumSamplesT ≤ NumSamples; if NumSamples > 10 then NumSamplesT=1.
- Perform Zero-Suppression as on https://twiki.cern.ch/twiki/bin/view/Main/HCalZeroSuppression
- Provide a lot of monitoring items over VME and to DCC
- Empty Events generation (with correct Ev#, BC# and Orbit#) when the FPGA is busy

FEATURES in HISTOGRAMMING MODE

- used for detector calibration with radioactive source
- works only if the FrontEnd does not send orbit messages

HTR board habitat



FE / HTR Data format

From: http://www-ppd.fnal.gov/tshaw.myweb/CMS/FE/Prod/FE_v3.pdf and http://cmsdoc.cern.ch/cms/HCAL/document/www-ppd.fnal.gov/tshaw.myweb/CMS/CCA/Prod/CCA_v5.pdf

Last bit transmitted [GOL Ref. Manual - Version 1.6 , page 8].

Timing of D(24) is not 100% proven. Timing of IDLE-to-DATA transitions is guaranteed.

In DATA mode, bits D(16) and D(0) are constant, they are both received as LSB by the HTR, and they allow to distinguish the two 16-bit half-words received.
NB: that is not true in IDLE mode (or with Errors).

	D(31:30)	D(29:25)	D(24)	D(23:22)	D(21:17)	D(16)	D(15:14)	D(13:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	QIE 0 Exp (1:0)	QIE 0 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 1 Exp (1:0)	QIE 1 Mant (4:0)	"0"	QIE 2 Exp (1:0)	QIE 2 Mant (4:0)	QIE 0 CapID(1:0)	QIE 1 CapID(1:0)	QIE 2 CapID(1:0)	Control Flag=0	Data Flag=1	"1"
Optical Cable 2	QIE 4 Exp (1:0)	QIE 4 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 5 Exp (1:0)	QIE 5 Mant (4:0)	"0"	QIE 3 Exp (1:0)	QIE 3 Mant (4:0)	QIE 4 CapID(1:0)	QIE 5 CapID(1:0)	QIE 3 CapID(1:0)	Control Flag=0	Data Flag=1	"1"

FE DATA FORMAT

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	Bunch Count A (0:6)	QIE_Reset (abort gap marker?)	Bunch Count A (9:11)	Bunch Count Error A	CapID Error A	"XX"	"0"	Bunch Count B (0:6)	Bunch Count A (7:8)	"XX"	Bunch Count B (7:8)	Control Flag=1	Data Flag=0	"1"

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:13)	D(12)	D(11)	D(10:9)	D(8:7)	D(6:3)	D(2)	D(1)	D(0)
Optical Cable 2	Bunch Count C (0:6)	QIE_Reset (abort gap marker?)	Bunch Count C (9:11)	Bunch Count Error C	CapID Error C	"XX"	"0"	Bunch Count B (9:11)	Bunch Count Error B	CapID Error B	"XX"	Bunch Count C (7:8)	"XXXX"	Control Flag=1	Data Flag=0	"1"

Supported: FE Orbit Message - Normal message

A word like this is preceded by a corrupted DATA word and followed by 69 IDLE words.

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:5)	D(4)	D(3)	D(2)	D(1)	D(0)
Optical Cable 1	Test Pattern "N" A(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" A(1:7)	"0"	Test Pattern "N" B(0:6)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XX"	Test Pattern "N+1" B(0)	Test Pattern "N" B(7)	Control Flag=0	Data Flag=1	"1"

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:2)	D(2)	D(1)	D(0)
Optical Cable 2	Test Pattern "N" C(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" C(7:1)	"0"	Test Pattern "N+1" B(7:1)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XXXX"	Control Flag=0	Data Flag=1	"1"

Treated as data: FE Orbit Message - Test Pattern message

Ten words like this are followed by 60 IDLE words (“C5BC” or “50BC”).

Updated 13JUL2009

HTR-DCC Data Format – FormatVer 5

From HTR version hex 886 (non-histogramming mode, non Empty-Event)

Word Type	S1 S0	Byte 1	Byte 0
HEADER	1 1	SR | Zeroes (overwritten by DCC)	EvN [7:0]
Ext. Header2	1 0	EvN [23:16]	EvN [15:8]
Ext. Header3	1 0	1 | CT | HM | TM | b11 | b10 | b9 | BE	CK | OD | LW | b4 | RL | EE=0 | BZ | OW
Ext. Header4	1 0	OrN [4:0] | HTR_sub_module_Number[10:0]	
Ext. Header5	1 0	FormatVer[3:0] = 5 | BCN[11:8]	BCN [7:0]
Ext. Header6	1 0	Total # of TP words[7:0].	NPS[4:0] # of PreSamples | DLLunlock[1:0] | TTCready
Ext. Header7	1 0	US | CM | Future | SubVersion [3:0]	HTR_Firmware_version[7:0]
Ext. Header8	1 0	0 | HTR flavor[6:0]	Pipeline-Length[7:0]
TP-DATA1	1 0	{TP_tag[4:0], Z, SOI, TP[8:0]}	
…	1 0	…	
TP-DATAm	1 0	{TP_tag [4:0]; Z; SOI; TP[8:0]}	
DAQ-DATA1	1 0	{FiberAd[2:0]; QIE-Ad[1:0]; Er; DV; CapID[1:0]; QIE-range[1:0]; QIE-mantissa[4:0] }	
…		…	
DAQ-DATAn	1 0	{FiberAd[2:0]; QIE-Ad[1:0]; Er; DV; CapID[1:0]; QIE-range[1:0]; QIE-mantissa[4:0] }	
Parity word	1 0	Insert a word “FFFF” if zero-sup leads to an odd # of data words	
Extra-Info1	1	The content of these 8 words depends on the value of the bits US and CM on Ext. Header7 See next pages	
Extra-Info2			
Extra-Info3	1 0		
Extra-Info4	1 0		
Extra-Info5	1 0		
Extra-Info6	1 0		
Extra-Info7	1 0		
Extra-Info8	1 0		
Pre-Trailer3	1 0	NS[4:0] =# of DaqData Samples (per L1A)	Total number of QIE words after ZS. 11-bit.
Pre-Trailer2	1 0	CRC[15:0] (DCC may replce this with Word-count)	
Pre-Trailer1	1 0	Zeroes (overwritten by DCC)	
TRAILER	0 1	EvN [7:0]	Zeroes (overwritten by DCC)

End of Life

See notes on next pages

Updated 17NOV2011

HTR-DCC Data Format – FormatVer 6

From HTR version 90_s2 = hex 290 (non-histogramming mode, non Empty-Event)

	S1 S0															
HEADER	1 1	**SR**	Zeroes (overwritten by DCC)							EvN [7:0]						
Ext. Header2	1 0	EvN [23:16]								EvN [15:8]						
Ext. Header3	1 0	1	**CT**	**HM**	**TM**	**b11**	**b10**	**b9**	**BE**	**CK**	**OD**	**LW**	**b4**	**RL**	**EE=0**	**BZ**	**OW**
Ext. Header4	1 0	5-bit OrN								11-bit HTR_sub_module_Number a.k.a. HTRsubmodN							
Ext. Header5	1 0	4-bit FormatVer = 6				BCN[11:8]				BCN [7:0]							
Ext. Header6	1 0	8-bit # of TP words after ZS, called M below								5-bit NumPreSamples			DLLunlock[1:0]		TTCready		
Ext. Header7	1 0	US	CM	Future		4-bit SubVersion				8-bit HTR fw version (a.k.a. CoreFPGAversionN)							
Ext. Header8	1 0	0	7-bit HTR flavor a.k.a. TypeN							8-bit PipelineLength							
TP-word 1	1 0	{TP_tag[4:0]; **Z**; SOI; TP[8:0]}															
…	1 0	…															
TP-word M	1 0	{TP_tag [4:0]; **Z**; SOI; TP[8:0]}															
QIE-word 1	1 0	**QIE-block data format. See next pages**															
…																	
QIE-word N	1 0																
Parity word	1 0	If needed, a word “FFFF” is inserted in order to have an even # of words															
Extra-Info1	1 0	The content of the 8 Extra-info words depends on the values of the bits US and CM on ExtHeader7. See next pages															
Extra-Info2	1 0																
Extra-Info3	1 0																
Extra-Info4	1 0																
Extra-Info5	1 0																
Extra-Info6	1 0																
Extra-Info7	1 0																
Extra-Info8	1 0																
Pre-Trailer3	1 0	5-bit NumSamples								11-bit number of QIE-words after ZS, called N above							
Pre-Trailer2	1 0	CRC[15:0] (DCC may replace this with Word-count)															
Pre-Trailer1	1 0	Zeroes (overwritten by DCC)															
TRAILER	0 1	EvN [7:0]								Zeroes (overwritten by DCC)							

See notes on next pages

QIE-block data format

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel-header	**1**	**Flavor[2:0]=5**			**ErrF[1:0]**		**CapId0[1:0]**		**ChannelId[7:0]**							
	0	Qie Sample 1							0	Qie Sample 0						
	0	Qie Sample …							0	Qie Sample <NumSamples-2>						
Channel-header	**1**	**Flavor[2:0]=6**			**ErrF[1:0]**		**CapId0[1:0]**		**ChannelId[7:0]**							
	0	Unused			Er, DV		CapId[1:0]		0	Qie Sample 0						
	0	Unused			Er, DV		CapId[1:0]		0	Qie Sample 1						
		Unused			Er, DV		CapId[1:0]		0	Qie Sample …						
	0	Unused			Er, DV		CapId[1:0]		0	Qie Sample <NumSamples-2>						

- NumSamples is an even number, with: 2 ≤ NumSamples ≤ 20 (The example in the table has
- ErrF[0] is asserted if there was a CapId violation (non correct rotation), related to the samples in the block, or if there are no CapIds (e.g. in Idle words)
- ErrF[1] is asserted if there was an asserted Link-Er , related to the samples in the block
- CapId0 is the CapId relative to Sample 0
- ChannelId[7:0] = {0, 0, 0, FiberId[2:0], QieId[1:0]}
- Qie Samples are 2-bit range plus 5-bit mantissa ("raw ADC values").
- The flavor = 6 has been introduced from HTR version 0x790 ("extended error" flavor).

Updated 1APR2012

The Extra-info words depends on the Ext. Header7 bits:

“Compact Mode” = **CM** , “UnSuppressed event” = **US**

Case CM=1 US=? (Compact Mode)

The 8 Extra-info words are not present

Case CM=0 US=0 (Normal Mode)

Word Type	Bits [15:12]	Bits [11:0]
Extra-Info1	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber1 IDLE, after pipeline [11:0]
Extra-Info2	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber2 IDLE, after pipeline [11:0]
Extra-Info3	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber3 IDLE, after pipeline [11:0]
Extra-Info4	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber4 IDLE, after pipeline [11:0]
Extra-Info5	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber5 IDLE, after pipeline [11:0]
Extra-Info6	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber6 IDLE, after pipeline [11:0]
Extra-Info7	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber7 IDLE, after pipeline [11:0]
Extra-Info8	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber8 IDLE, after pipeline [11:0]

Case CM=0 US=1 (UnSuppressed data: a mark bit is set if the channel would have been normally suppressed)

Word Type	Bits [15:0]	
Extra-Info1	marks for TP-channels 8 down to 1	marks for digi-channels 8 down to 1
Extra-Info2	marks for TP-channels 16 down to 9	marks for digi-channels 16 down to 9
Extra-Info3	marks for TP-channels 24 down to 17	marks for digi-channels 24 down to 17
Extra-Info4	threshold of digi-ch24 (8-bit)	threshold of digi-ch1 (8-bit)
Extra-Info5	ThresholdTP[3:0]	Synchronization-Fifo Count[2:0] for fibers: 4, 3, 2, 1
Extra-Info6	ThresholdTP[7:4]	Synchronization-Fifo Count[2:0] for fibers: 8, 7, 6, 5
Extra-Info7	0 ZS_Mask[18:16]	BCN-of-RxBC0 (12-bit)
Extra-Info8	ZS_Mask[15:0]	

Updated 1AUG2009

HTR-DCC Data Format

non-histogramming mode, Empty-Event

Word Type	S1 S0	**Byte 1**	**Byte 0**
HEADER	1 1	**SR** Zeroes (overwritten by DCC)	EvN [7:0]
Ext. Header2	1 0	EvN [23:16]	EvN [15:8]
Ext. Header3	1 0	1 **CT** **HM** **TM** **BE**	**CK** **OD** **LW** **LE** **RL** **EE=1** **BZ** **OW**
Ext. Header4	1 0	5-bit OrN	11-bit HTR_sub_module_Number a.k.a. HTRsubmodN
Ext. Header5	1 0	4-bit FormatVer BCN[11:8]	BCN [7:0]
Pre-Trailer2	1 0	CRC[15:0] (DCC may replace this with Word-Count)	
Pre-Trailer1	1 0	Zeroes (overwritten by DCC)	
TRAILER	0 1	EvN [7:0]	Zeroes (overwritten by DCC)

The empty-event condition prevails on the unsuppressed event condition.
In the case of an Empty-Event, the bit US is not reported. So any software that unpack the data and search for the US bit should look only non empty-events (EE=0).

See notes on next pages

Notes about the HTR/DCC data format

Information relevant to DCC in the first and last 3 words. DCC puts Ext. Header3 [8:0] in the Common Data Format

SR = Status Request (from a TTC command, for the DCC LRB)

EvN = Counted internally. It should be = TTCrx EvN + 1. Does not count VME triggers.

OW= Overflow Warning. See another page in this document. If L1A rate is reduced the HTR should not go Busy.

BZ = Internal buffers Busy; not necessarily related to the current data block. Fast monitoring, it could be reported to the aTTS by the DCC.

EE = Empty Event (consequence of a past BZ). An **Empty Event** includes only the first 5 header words and the last 3 words. CMS spec.

RL = Rule violated by L1A (it refers to trigger rules i and ii of Trigger TDR 16.4.3)

b4 = bit asserted if FE idle or corrupted words have been triggered. These FE words may have been suppressed.

LW = bit asserted if "Jose" Latency-Fifo has tuned the latency since the previous block transmission.

OD = Optical Data error: this is a monitoring information. Logic "OR" of all possible errors (link, format, CapID) on all non-masked QIE-channels. Reset after each HTR event. It does not indicate a bad event; it simply monitor the links.

CK = An "OR" of clocking problems (~TTCready, DLL_unlock). If set, the event should not be considered good.

BE = Bunch Error: asserted if BCN does not wrap around correctly when BC0 is received.

TM = Test Modes: can be CounterMode or PatternMode: if "0" real data; if "1" test data. L1As needed as in the real mode. Set from VME.

HM = Histogramming mode, need to change firmware to switch. It is a 0 in normal mode.

CT = Calibration Trigger event if 1 (L1A event if 0);

US = UnSuppressed data block (a.k.a. NZS or M&P) : Zero-Suppression is not performed on this event.

SOI = Sample Of Interest: it is the (NumPresamplesT)-th sample of TP-word.

Z = if "1", it means that the value of TP[8:0] sent to the SLB and RCT was zero (i.e. was not a peak).

DLL_unlock[1:0] =It counts how many times the DLL unlocked since last Hard_rst, not tested.

BCN[11:0] = BCN at the time the trigger corresponding to the current data block arrived to the HTR.

(Er, DV) : if (0, 0) means IDLE; if (0, 1) means non-corrupted data; if (1, X) means error.

Information on the TP_words

For HBHE, HF: TP_tag[4:0] = { SLB_ID[2:0]; SLB_ch[1:0] } - repeated "NumSamplesT" times; where:
SLB_ID= 1, 2,…, 6; SLB_ch = 0, 1, 2, 3 ⇔ A0, A1, C0, C1 for top FPGA; B0, B1, D0, D1 for bottom FPGA.

For HO: TP-word = 00000 Z PS 0 muon_bits[8: 1] - repeated "NumSamplesT" times
00001 Z PS 0 muon_bits[16: 9] - repeated "NumSamplesT" times
00010 Z PS 0 muon_bits[24:17] - repeated "NumSamplesT" times

HTR-DCC Data Format
May 2005 - from HTR h6 (histogramming mode)

Word Type	**S1 S0**	**Byte 1**	**Byte 0**
HEADER	1 1	**SR** Zeroes	EvN [7:0]
Ext. Header2	1 0	EvN [23:16]	EvN [15:8]
Ext. Header3	1 0	1 **CT** **1** **TM**	**CK** **OD** **LW** **LE** **RL** **EE** **BZ** **OW**
Ext. Header4	1 0	OrN [5:0] HTR_sub_module_Number[9:0]	
Ext. Header5	1 0	FormatVer[3:0] BCN[11:8]	BCN [7:0]
Ext. Header6	1 0	0 HistFib2[2:0] 0 HistFib1[2:0]	DLL_unlock[1:0] TTCready
Ext. Header7	1 0	Firm. vers. #[18:16] HTR Firmware version Number[12:0]	
Ext. Header8	1 0	Reserved (0…0)	FiberError[7:0]
TP-DATA1	1 0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
…	1 0	…	
TP-DATAm	1 0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
DAQ-DATA1	1 0	{FiberAd[2:0]; QIEAd[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
…		…	
DAQ-DATAn	1 0	{FiberAd[2:0]; QIE Ad[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
Parity word	1 0	Insert a word “FFFF” if zero-sup leads to an odd # of data words	
Extra-Info1	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber1 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber2 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber3 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber4 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber5 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber6 Orbit Message [11:0]
	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber7 Orbit Message [11:0]
Extra-Info8	1 0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber8 Orbit Message [11:0]
	1 0	NS[4:0] =# of DaqData Samples (per L1A)	Total number of Daq words[10:0] after zero-sup.
	1 0	Reserved	WordCount[11:0]
Pre-Trailer	1 0	Zeroes	Zeroes
TRAILER	0 1	EvN [7:0]	Zeroes

FiberError[7:0] = 1 bit error summary per fiber. HistFib*[2:0] = which of the 8 input fibers is used for histogramming

Optical Scheme

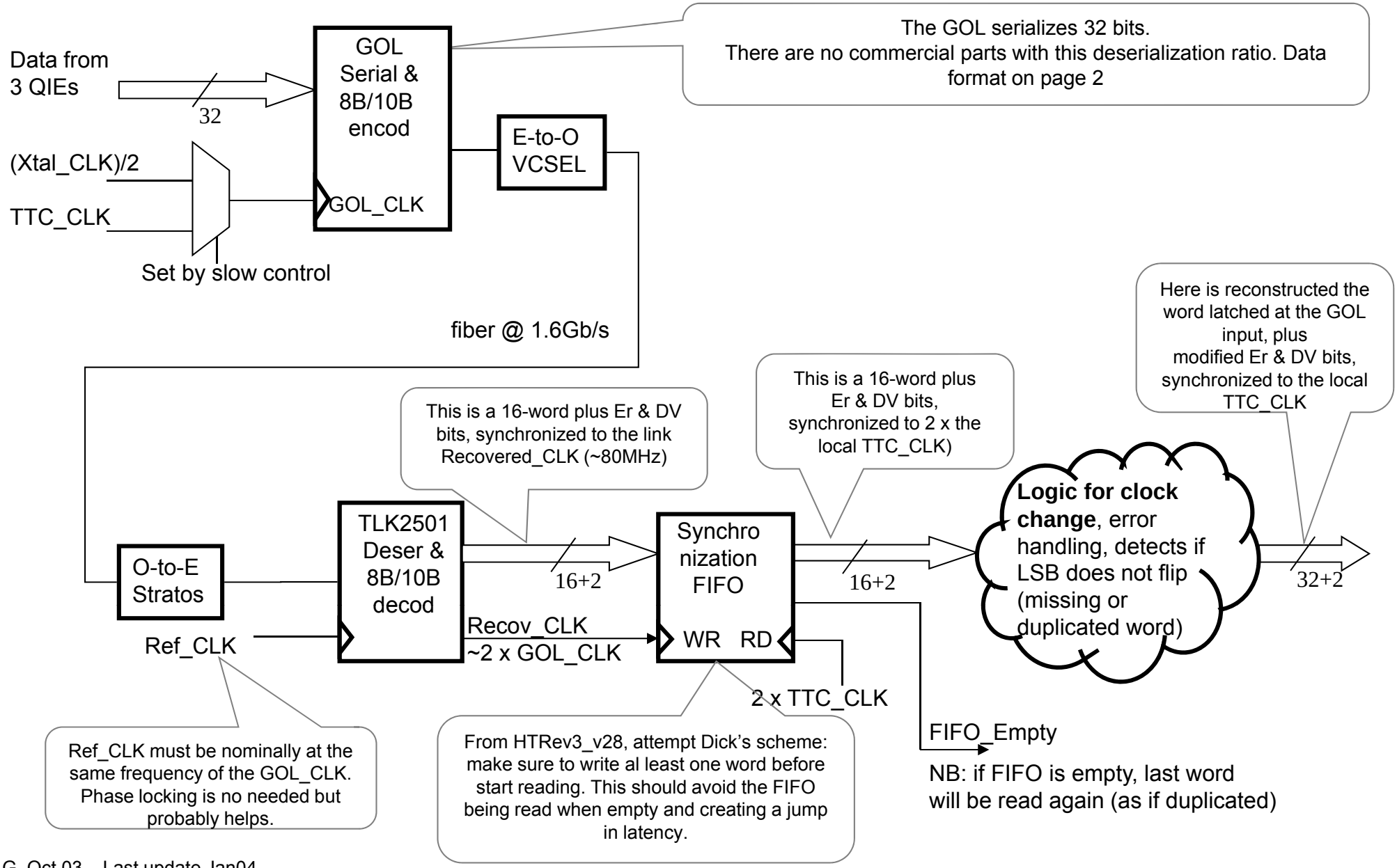
Date: Thu, 10 Jul 2003 11:05:50 -0500 (CDT)
From: Julie Whitmore <jaws@fnal.gov>
To: Tullio Grassi <tullio@Glue.umd.edu>
Cc: Drew Baden <drew@physics.umd.edu>, tshaw@fnal.gov Subject:
Re: fiber optic diagram

In the real system, the number of connections is somewhat larger than in the test beam. See my ESR presentation pages 21 & 22 http://www-ppd.fnal.gov/tshaw.myweb/CMS_Optical_Links.html (link to pdf file is at the bottom of the page)
[...]
In the real system, we have the following pieces (see ESR pp. 21&22):
1)Octopus inside RM (VCSEL to RM front panel)
2)Ribbon to patch panel [~20m] (fans-out at patch, but no fiber break)
3)Octopus inside patch panel (where channels are mapped)
4)Ribbon trunk to HTR [~70m]
5)Octopus on HTR
So the connections are
1)coupling to VCSEL, 2)coupling at RM front panel, 3)coupling at front of patch panel, 4)coupling at back of patch panel,
5)coupling at HTR front panel, 6) coupling to receiver.
The largest number of connections is with the calibration modules, where for some fibers we will have additional connections near the HTRs to try to fully populate the ribbon fibers. This is also true for the overlap regions of HB/HE, where we will have an additional patch panel to complete the mapping. I believe that adds an 2 extra connections (for the front and back part of the extra patch panel). So in the worst regions, we can have up to 8 connections. As for attenuation, the typical attenuation is 0.5dB per connection. The fiber attenuation is 2.5dB/km or 0.25dB for 100m. So we an exptect up to 3.25-4.25dB for the real system. Terri made a measurement with 10 connections and 150m of fiber. She measured 7.3dB attenuation, but she also had a 62.5um connection to her optical probe (fibers are 50um), where she said she expected to lose an additional ~3dB from her setup. So we expected 5.4dB and measured ~4.3dB (7.3dB - 3dB (for probe)). I hope this information helps. –julie
==========
Date: Fri, 19 Dec 2003 16:37:40 -0600 (CST)
From: Julie Whitmore <jaws@fnal.gov>
To: Tullio Grassi <tullio@Glue.umd.edu>
Cc: Drew Baden <drew@physics.umd.edu>, Theresa Shaw <tshaw@fnal.gov>
Subject: Re: summary of tests
[CUT] I spec'd 50/125 graded-index multimode, which means that there is not an index of refraction interface at the core boundary (variable index of refraction out to 125um).[CUT] The fiber is Germanium doped Silicon.

Next pages contain details of the design.

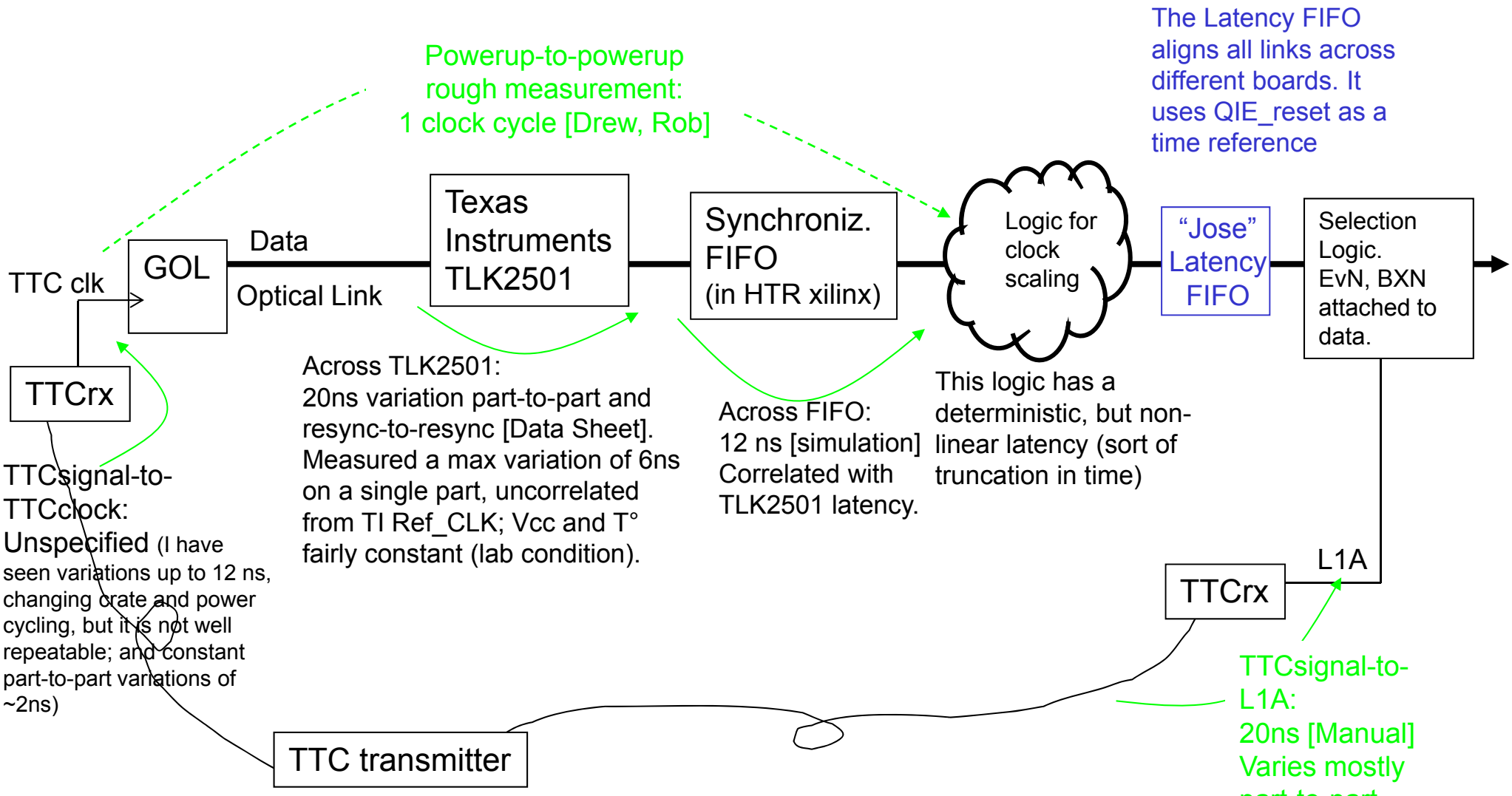
They can be useful to interpret the HTR behavior and the FPGA design (“firmware”).

FE-link logic diagram

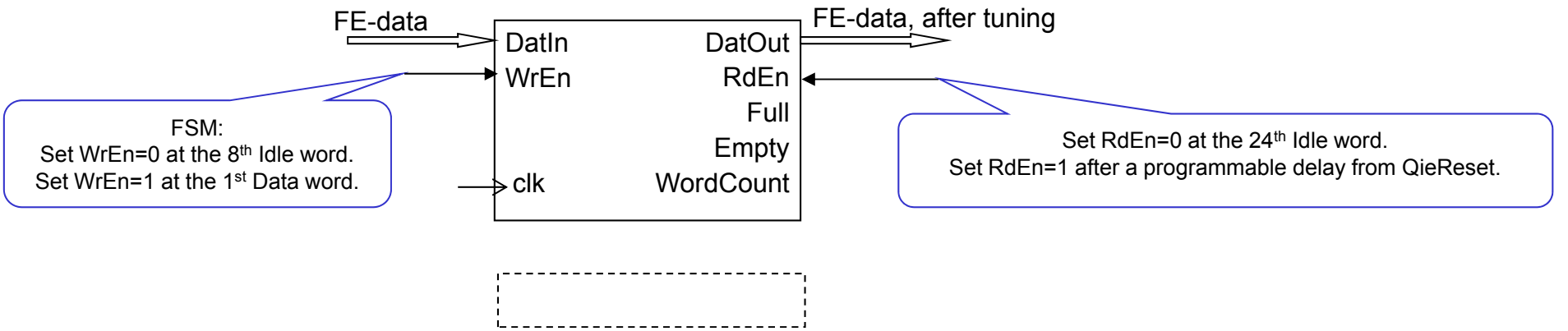


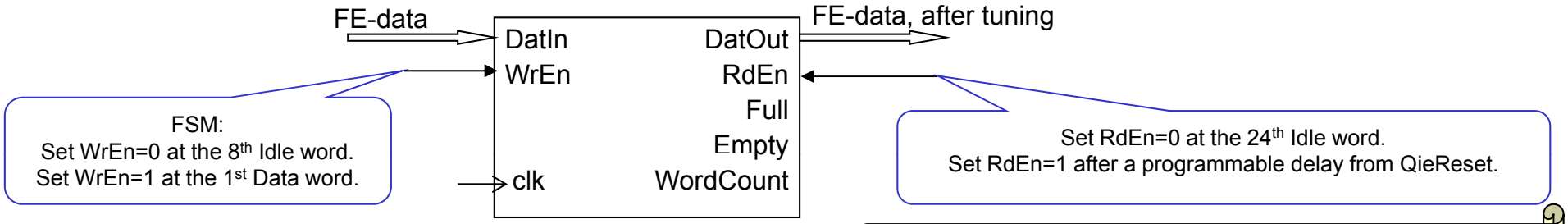
Random Latency in HCAL electronics

- Only components with a random latency are sketched -



Latency tuning with “Jose” Latency-FIFO

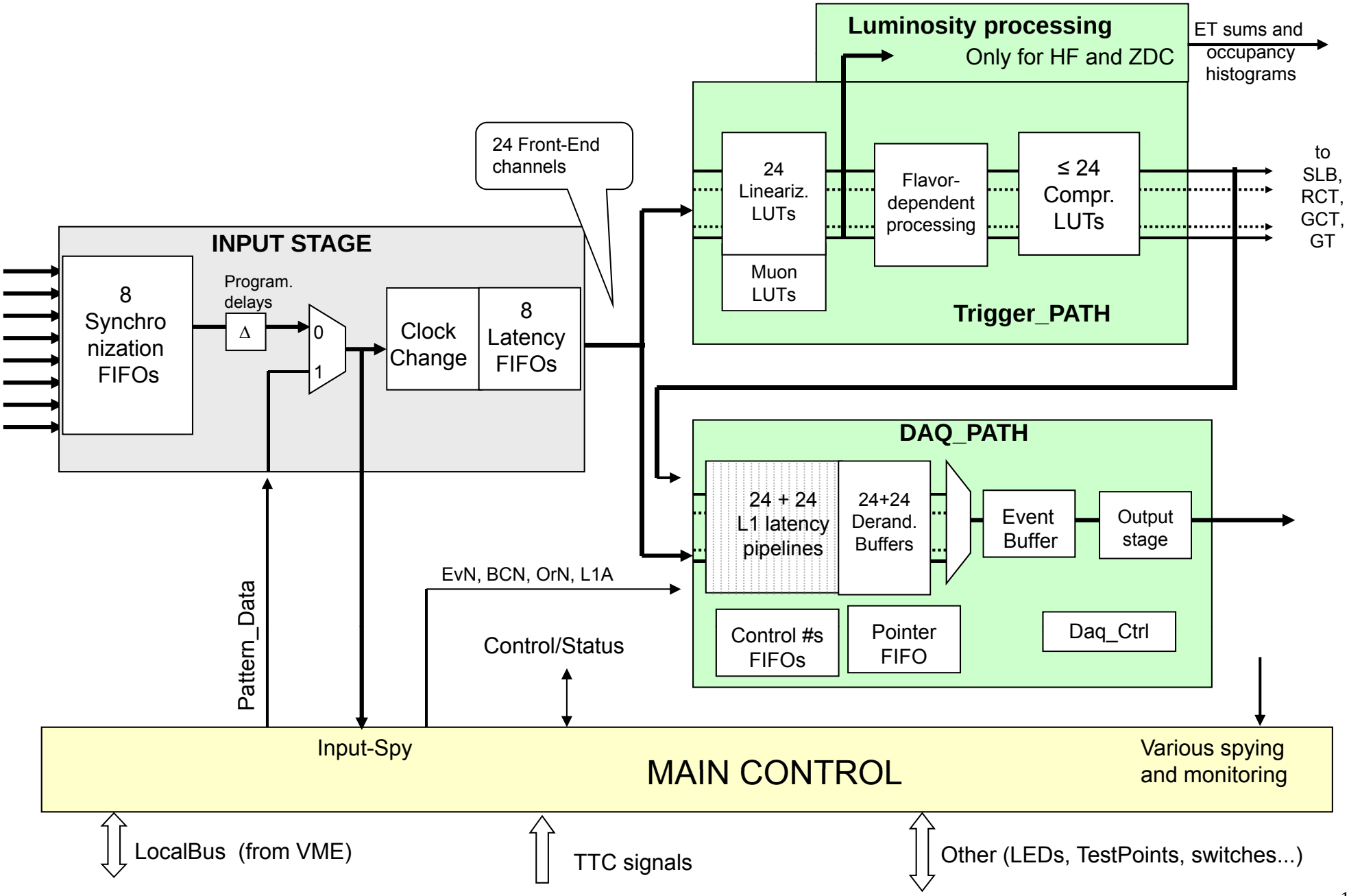




Idle timing can be different from link to link. So is the timing of WrEn, in order to capture the relevant words.

The timing of RdEn going “1” is the same for all links, across different boards and crates → latency tuning

HTR Main FPGA – top level

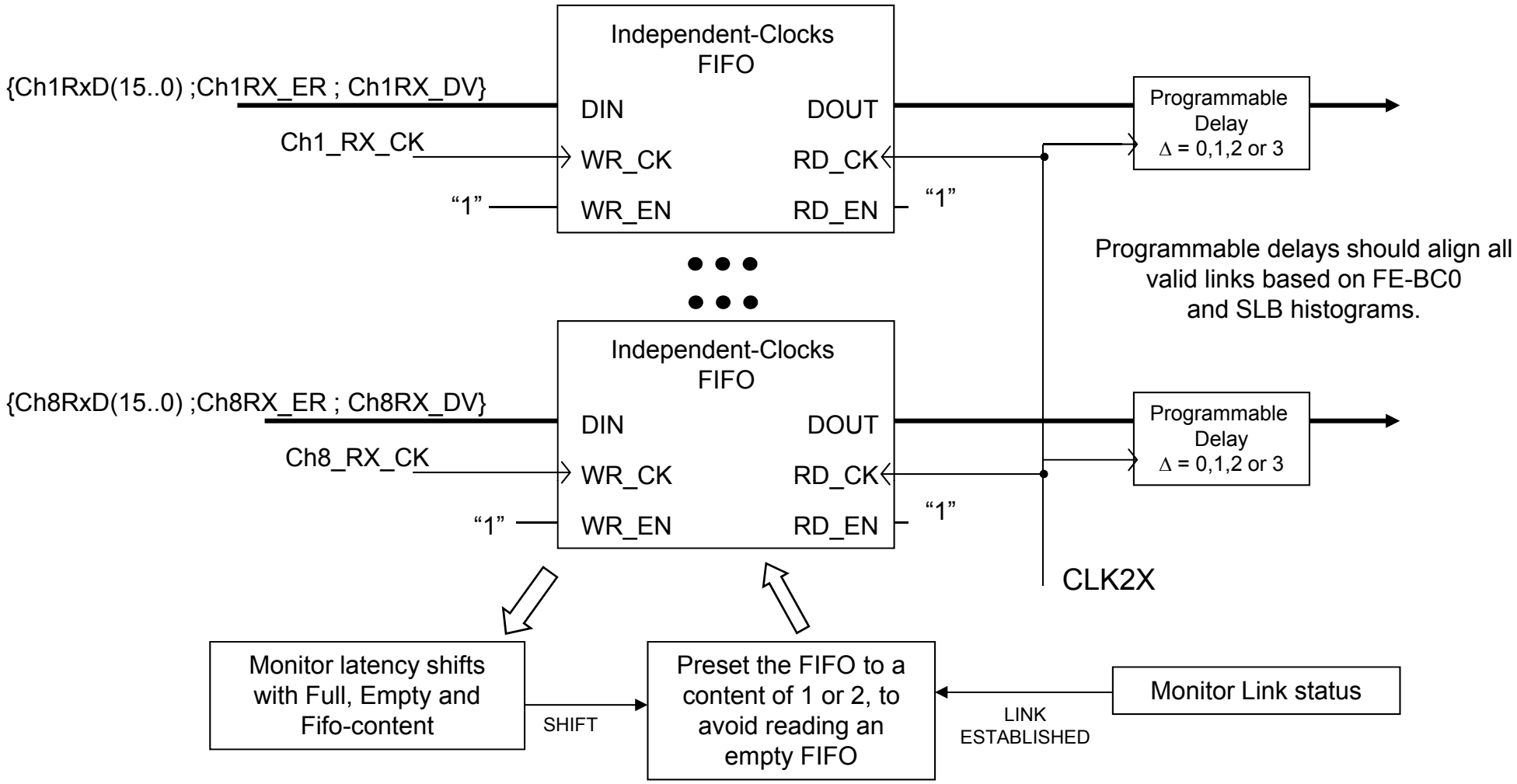


Synchronization FIFOs and Prog. Delays

Each incoming FE-bus is synchronous with its own Recovered_CK. This stage synchronizes the data to the System Clock x 2.
Consider the “Self-Addressing” architecture for these FIFOs (improve timing uncertainties).

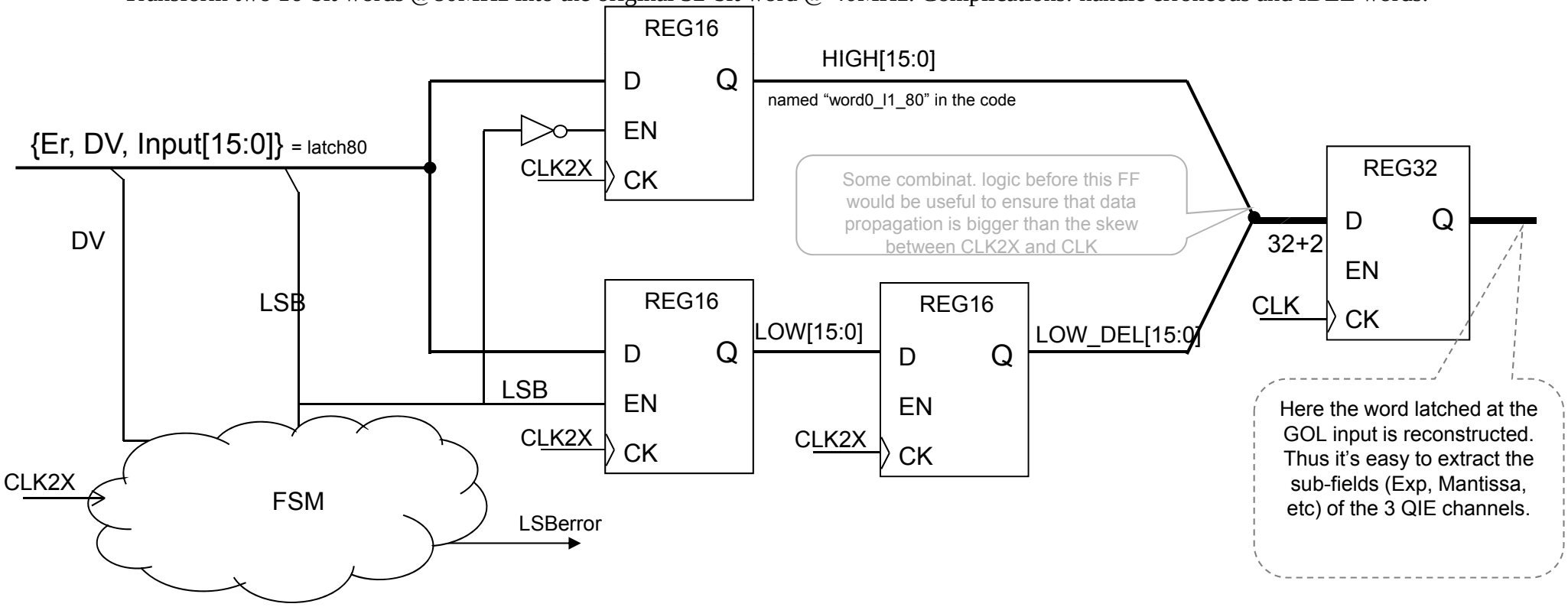
To align TPG data, a delay must be added to the corresponding channel. This value of each delay is the value of the gaps on the synchronization histogram. [Jose Carlos].

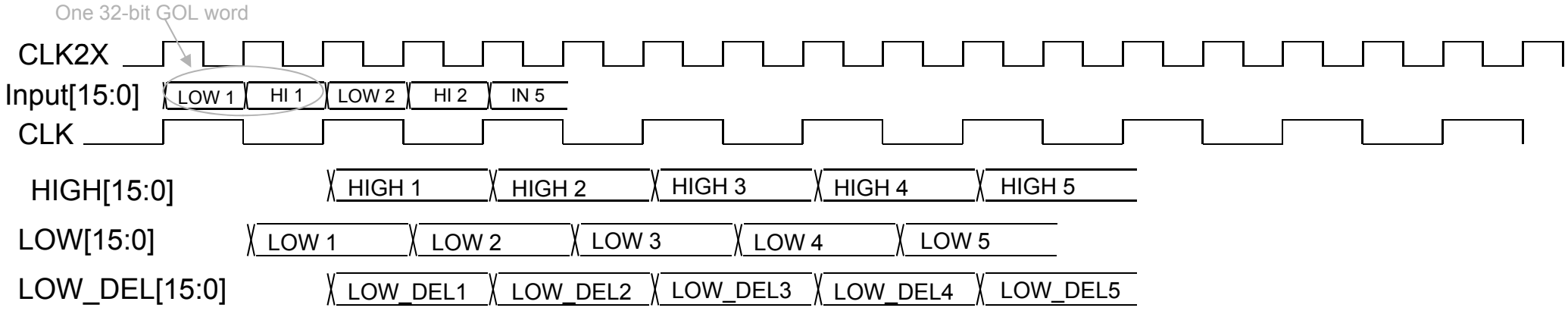
Make sure that when the link is down there is a free-running RX_CK from the TLK2501, in order to write ER and DV.



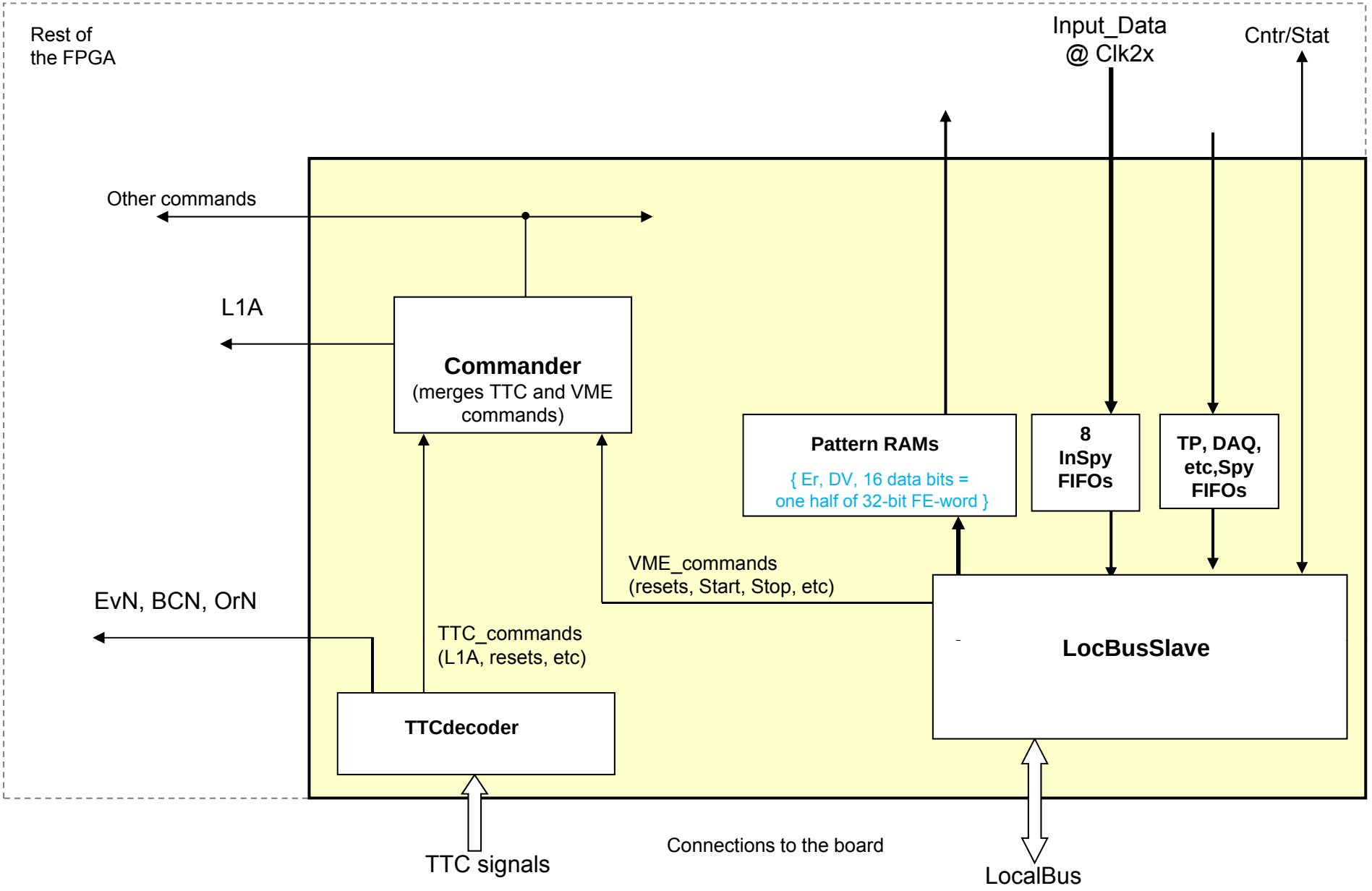
Clock Change stage (simplified)

Transform two 16-bit words @80MHz into the original 32-bit word @ 40MHz. Complications: handle erroneous and IDLE words.



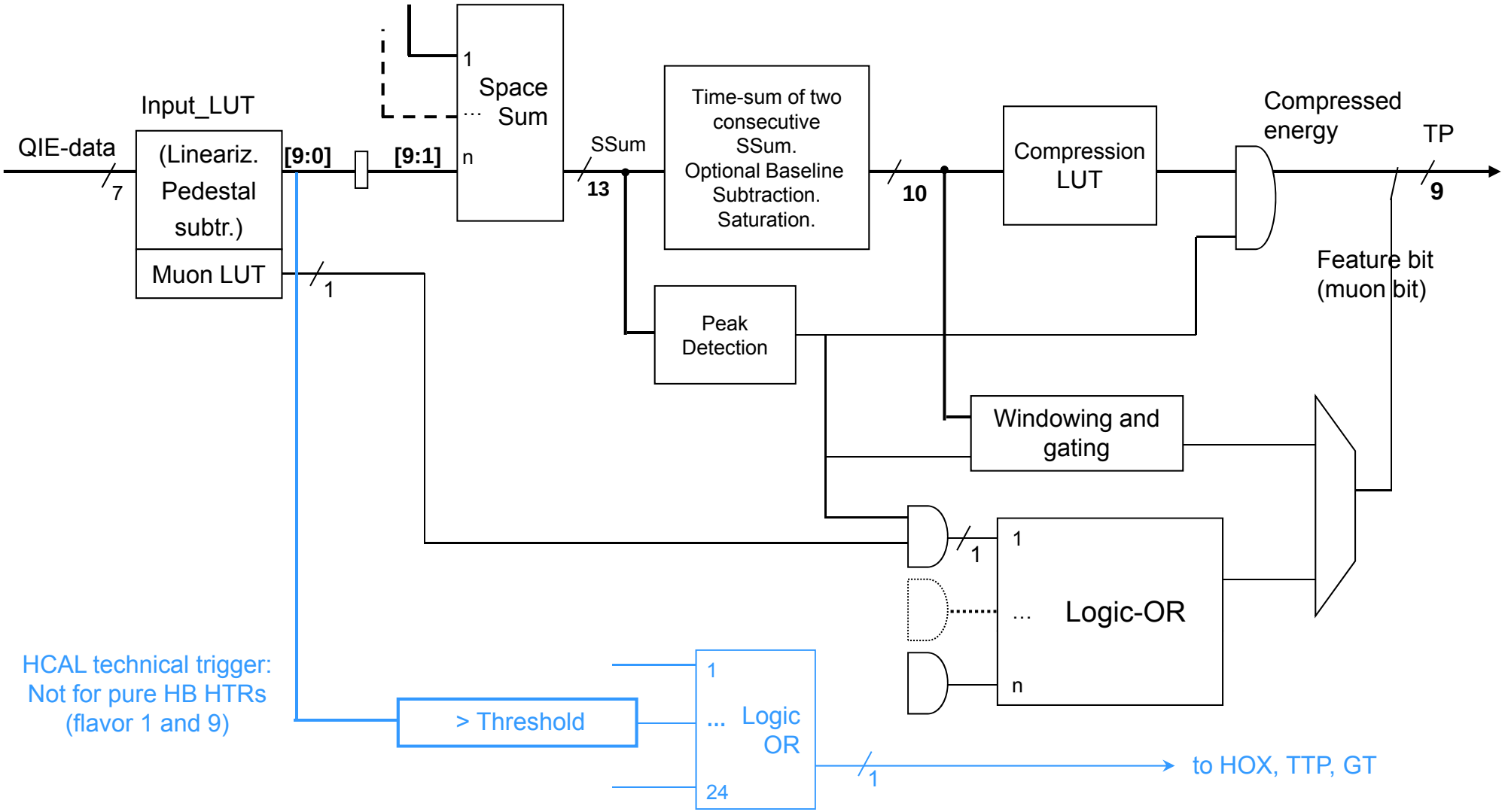


Control module of Main FPGA - MAIN_CNTR



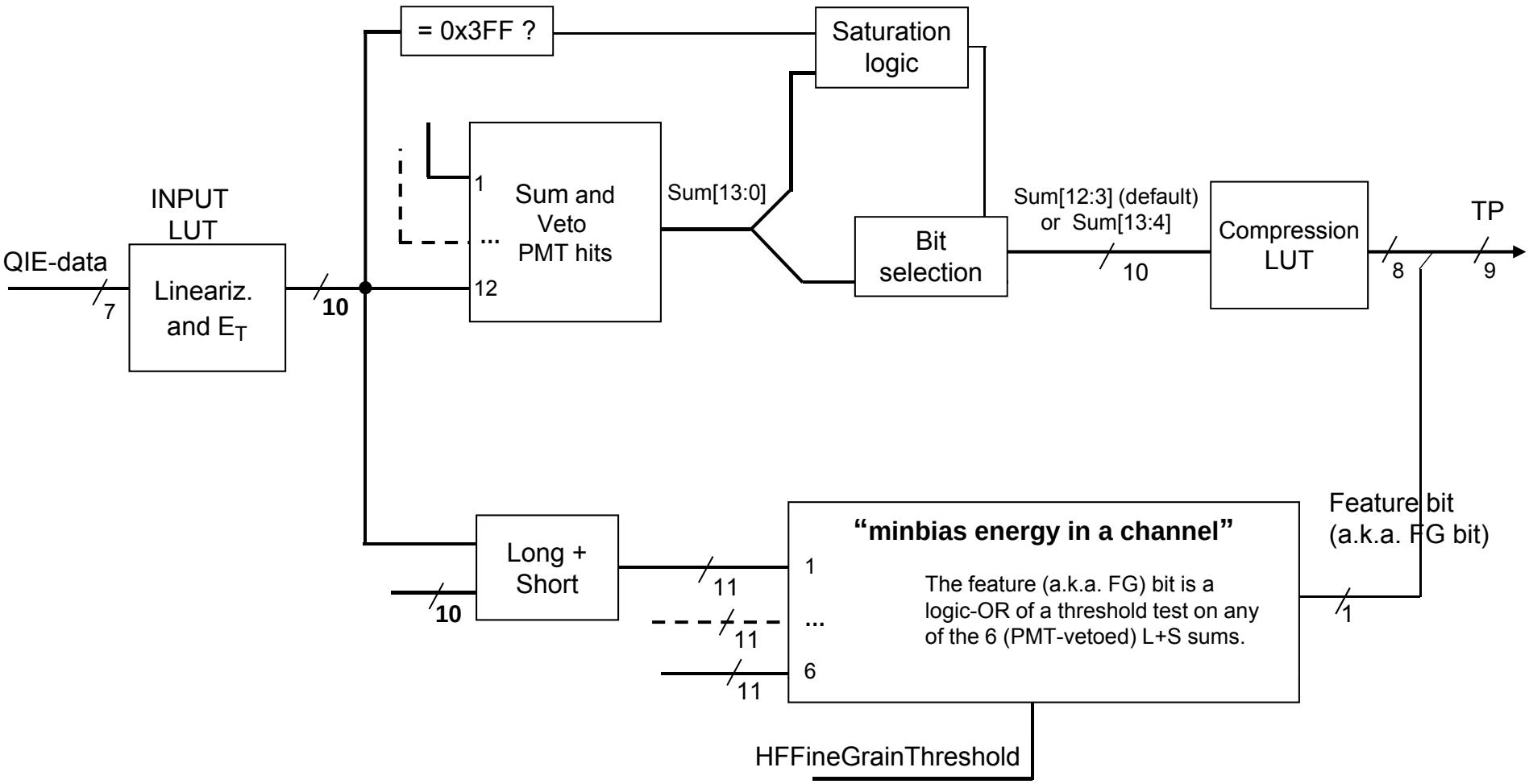
HB HE Trigger-Path:

Sum of n QIE-channels; n = 1, 2, 3, 5. April 2010; HTR version 0x689



The «Peak Detection» chooses the two-sample-sum of the largest sample and the following sample. If the sampling phase is fine, this should be the largest sum.
Each channel participating on the sum must have the possibility to be masked, to perform a sync histogram based on each independent channel (input data from each deserialiser) [J.C. Da Silva]
There is a unique Compression LUT for a group of n channels, where n can be 1, 2, 3, 5.

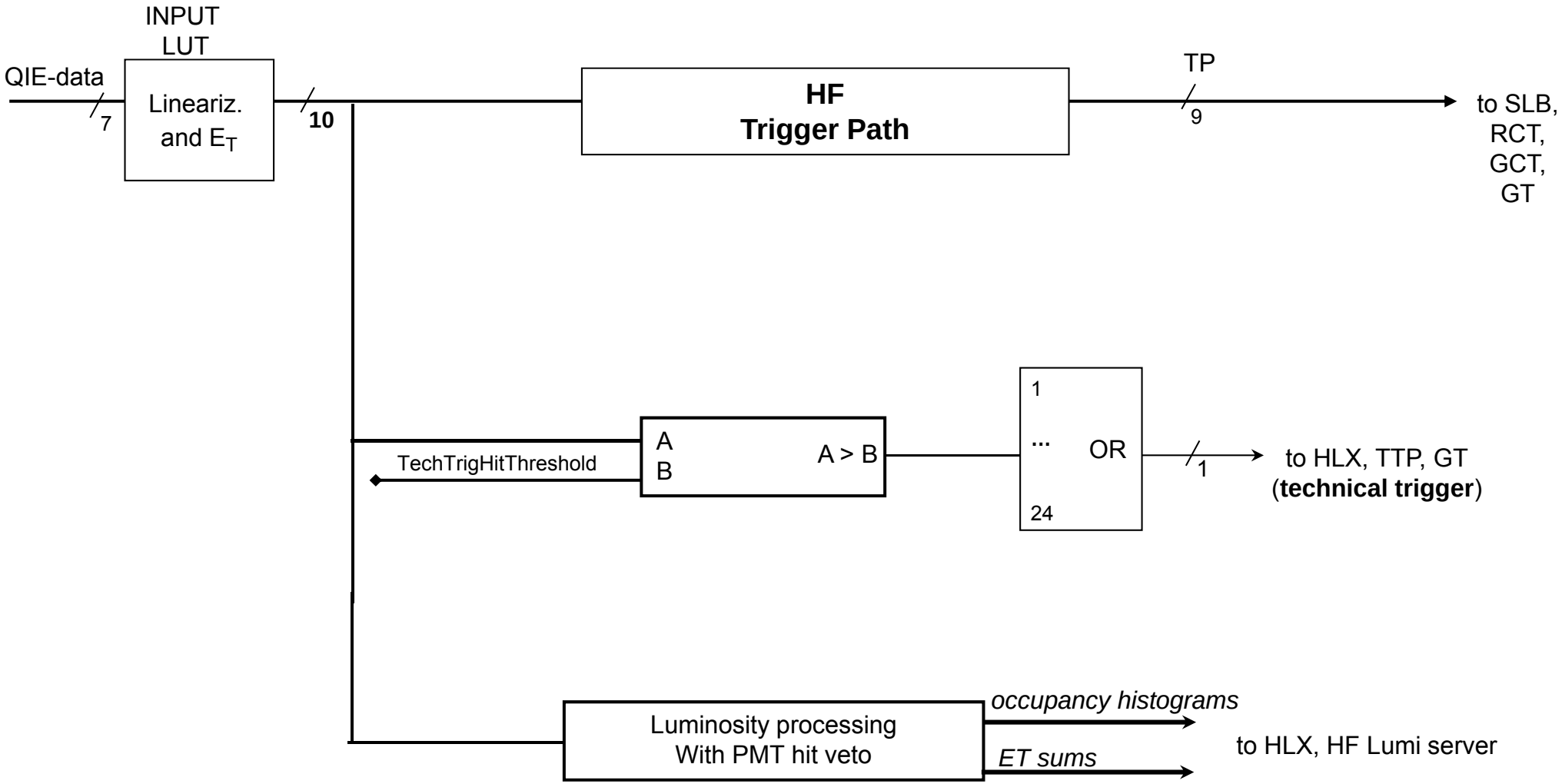
HF Trigger Primitive Generator - Feb 2011; HTR version 0xD89



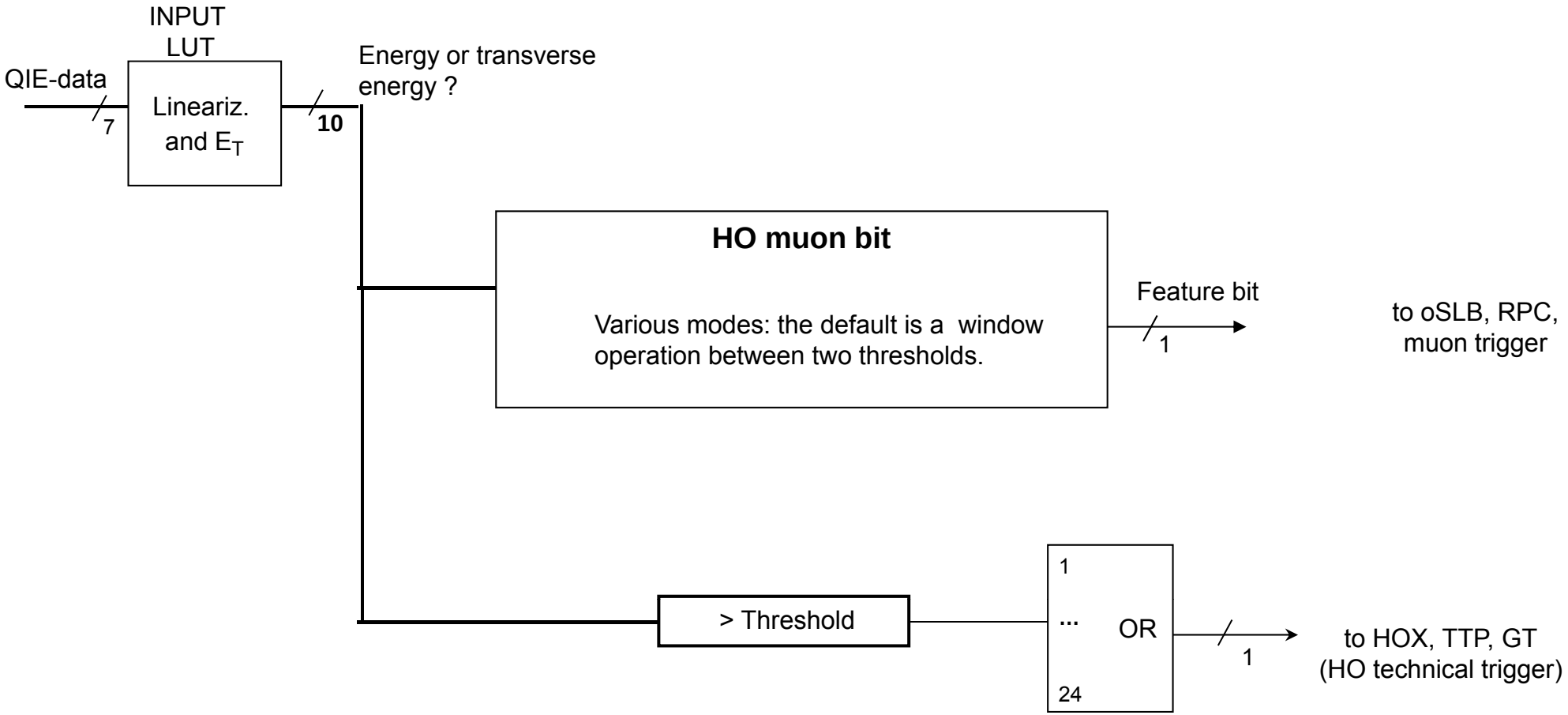
•Each channel participating on the sum must have the possibility to be masked, to perform a sync histogram based on each independent channel (input data from each deserialiser) [J.C. Da Silva]

HF: TPG, Technical Trigger, Lumi Processing -

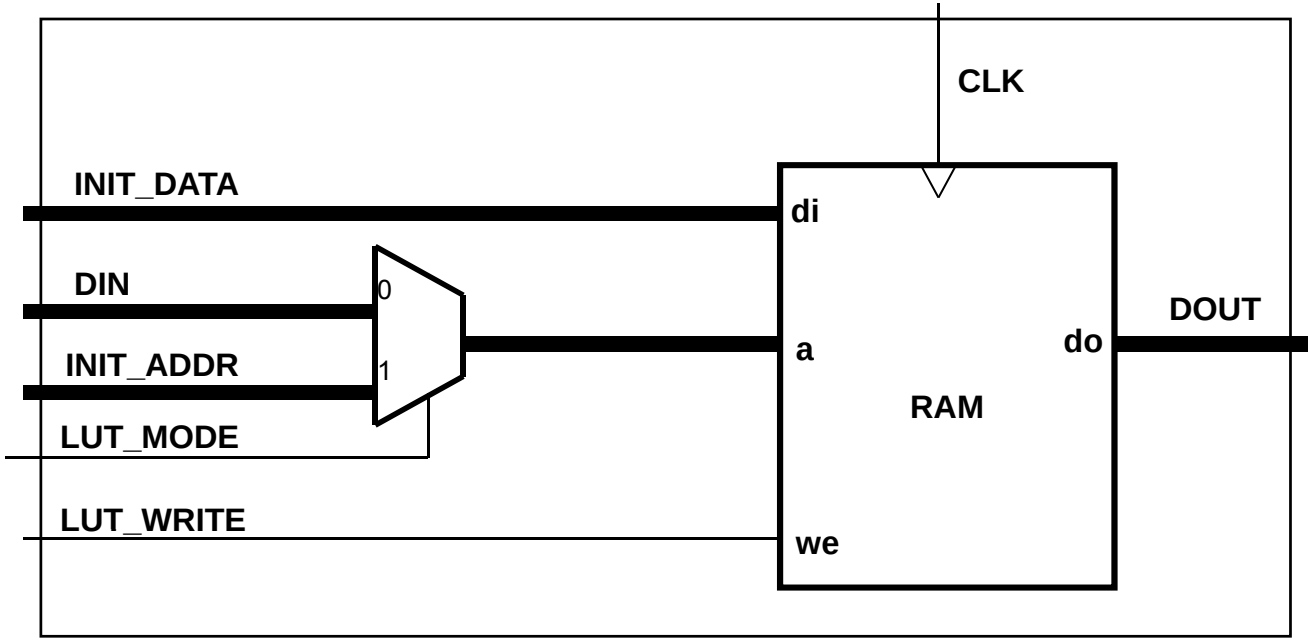
April 2010; HTR version 0x689



HO Trigger-Path - as of Sept 2008; version 84

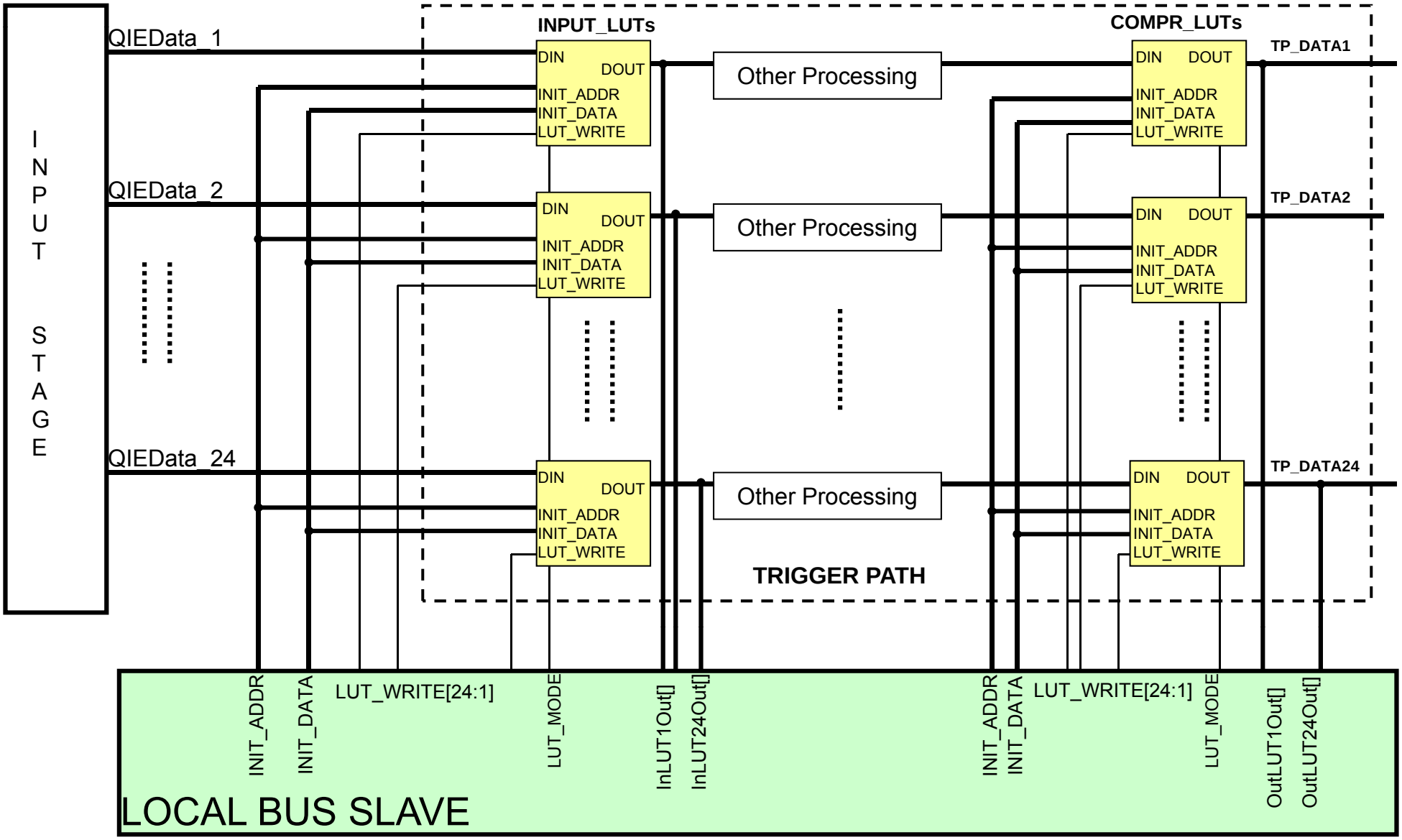


TPG LUTs



NB: during configuration this LUT has non-zero outputs, so need to disable (Stop command) the SLB board (software specification). During configuration, LUT Output data is not set to zero in the HTR Main FPGA in order to reduce the latency.
Impact on LUMI !?!

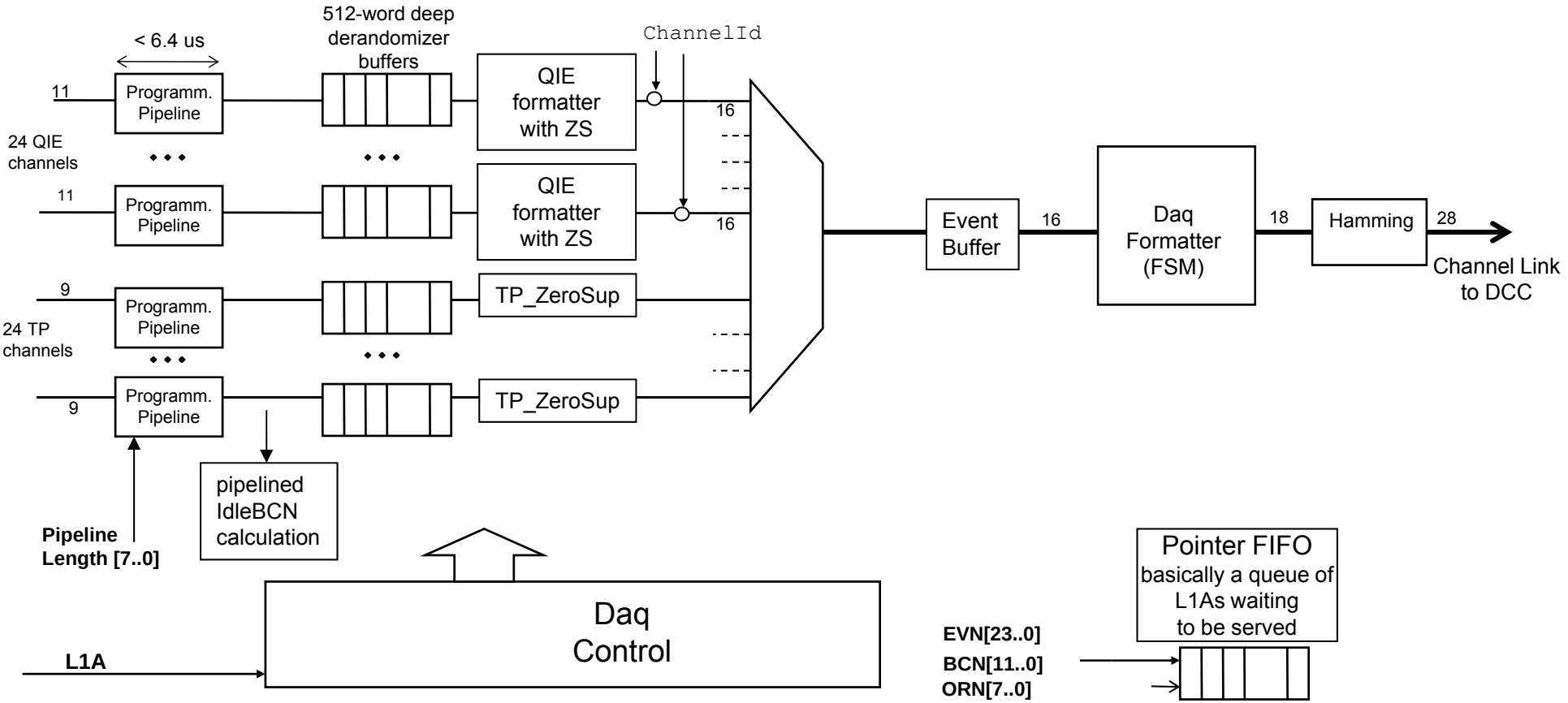
LUT Initialization Scheme over VME-Local Bus



NB: to configure a given LUT, from VME the access will be always at the same address. Then on the board VME FPGA the correct address will be generated with a counter.

L2-DAQ Path

No energy extraction algorithm ⇒ QIE-data + address.
The 24 QIE-channels, in parallel with the TP-channels are temporarily stored in a pipeline (circular buffer) to wait for the L1A trigger decision. The storage time is programmable between 0 and 255 clock ticks. Each L1A trigger selects a block of time-samples per QIE-channel and energies per TP-channel. The selected data of the 24 channels must be inserted on the HTR/DCC data format. EV#, BC#, ORBIT# must correspond to the appropriate data block.
Zero Suppression is described on: https://twiki.cern.ch/twiki/bin/view/Main/HCalZeroSuppression

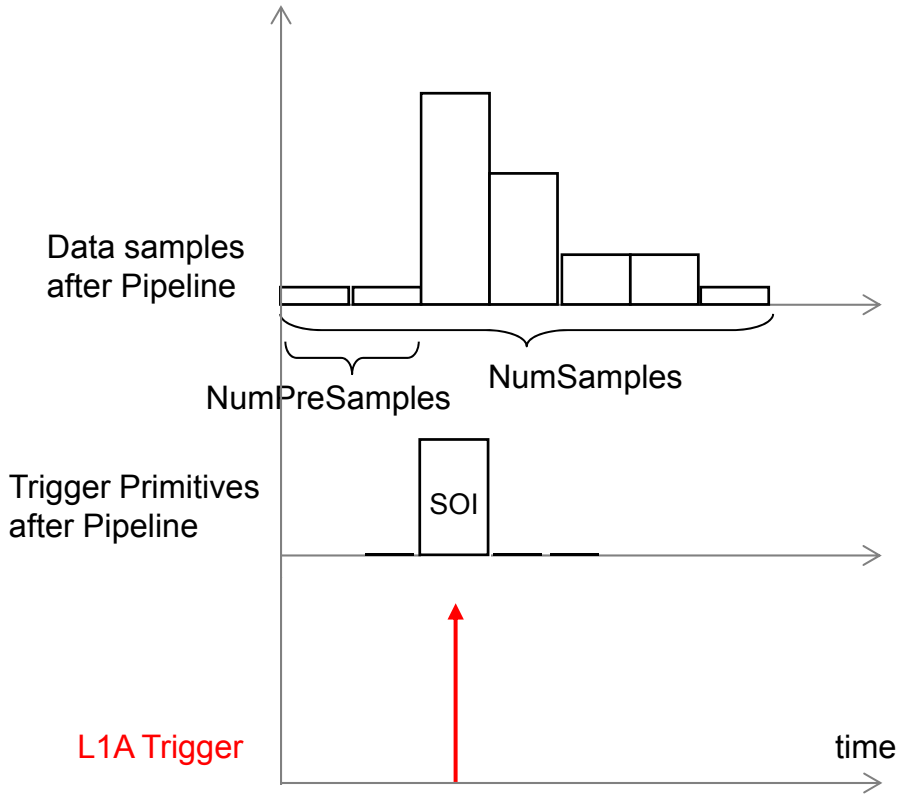


Alignment of QIE-Data and Trigger Primitives with the L1A Trigger

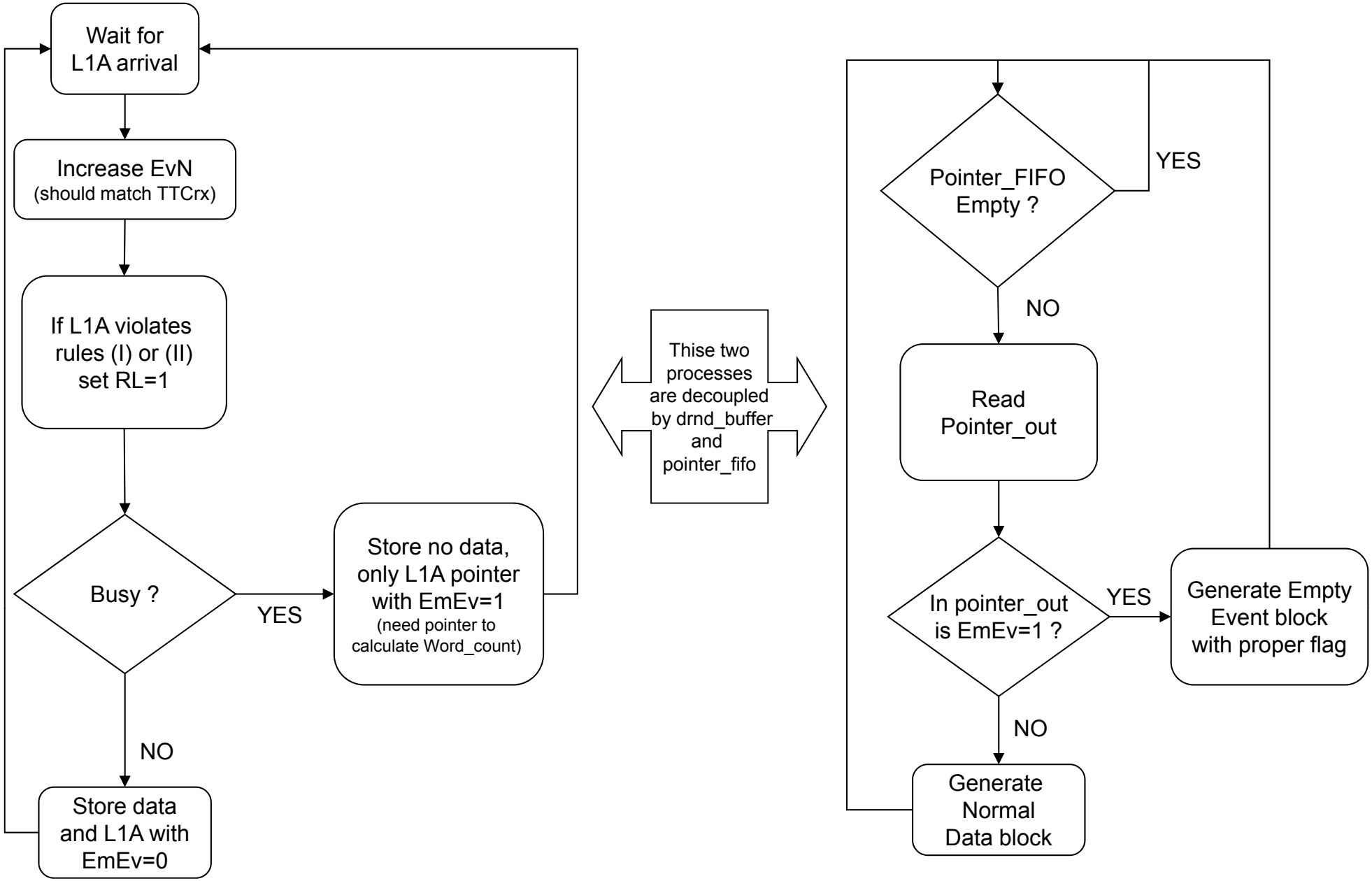
Parameters that can be set over VME, during run-configuration, in order to acquire the desired data:

NumSamples = Number of QIE-Data Samples
NumPresamples = Number of Pre-Samples
NumSamplesT = Number of Samples of TPs
NumPresamplesT = Number of Pre-Samples of TPs
PipelineLength = Length of the latency pipeline, i.e. a programmable delay applied on the Data Samples and on the Trigger Primitives.

The clock cycle (bunch crossing) corresponding to the arrival of the L1A is labeled SOI (Sample Of Interest).

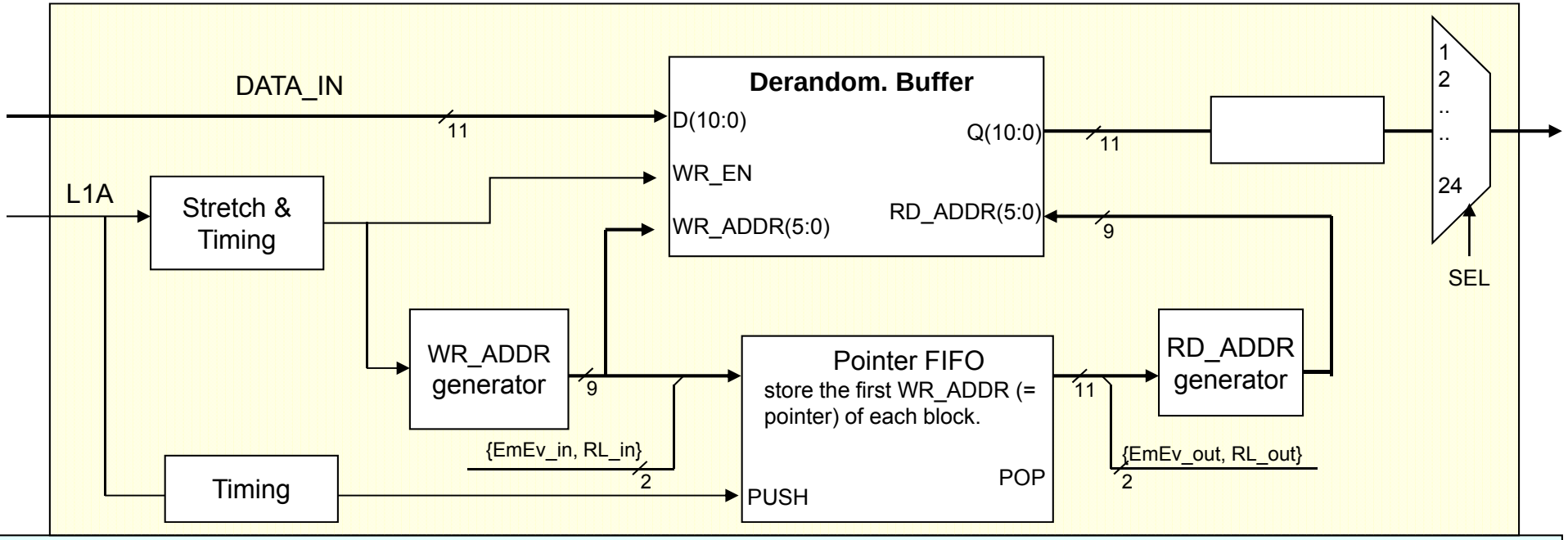


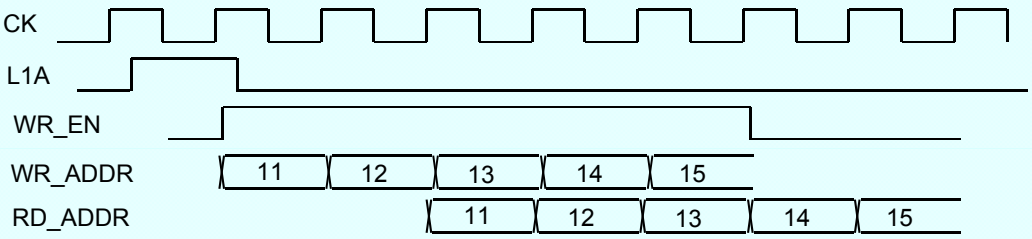
Trigger acceptance & Empty events



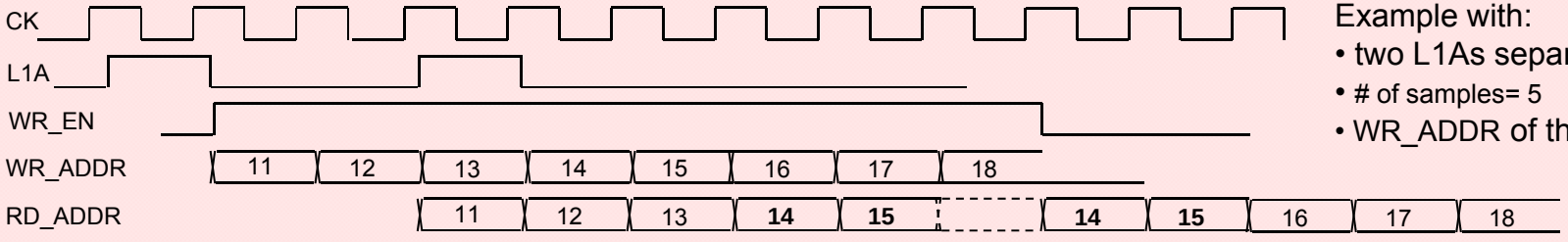
Derandomizer and trigger rules

The Derandomizer is not a simple FIFO as it handles the case of two L1A within a 4-tick interval (Trigger TDR 16.4.3).
Such an interval is smaller then the number of time samples (≈ 10) to be collected (Trigger TDR 7.3.1), thus overlapping.





Example with:
- # of samples = 5
- WR_ADDR of the first word = 11



Example with:
- two L1As separated by two BXs
- # of samples= 5
- WR_ADDR of the first word = 11

Overflow Warning (OW) and Busy (BZ) flags

Derandomizer buffers are 512-word deep RAMs. They are the first elements that can overflow in the HTR, in case of a high trigger rate.
Let: *word_count = drnd_wr_addr – drnd_rd_addr = number of words in the buffer*

There is a sort of hysteresis, to avoid that the flags keep toggling when the buffer are near a threshold:

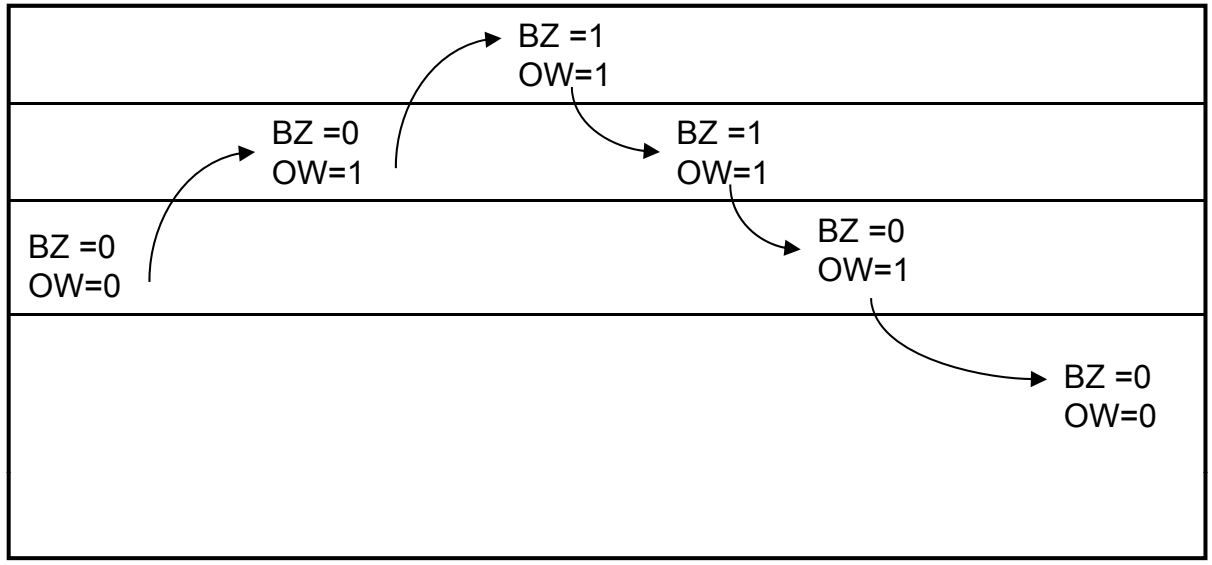
word_count = 512 (full)

word_count = 409 (80%)

word_count = 307 (60%)

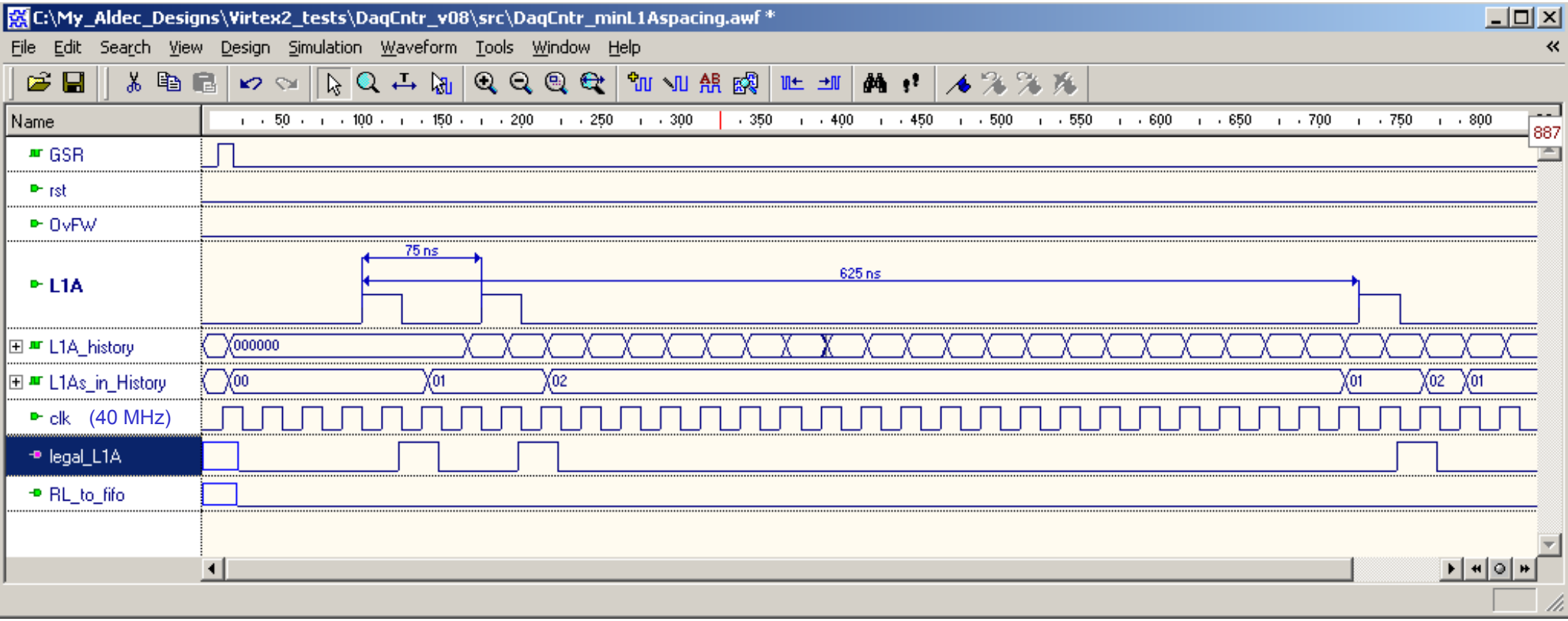
word_count = 256 (50%)

word_count = 0 (empty)



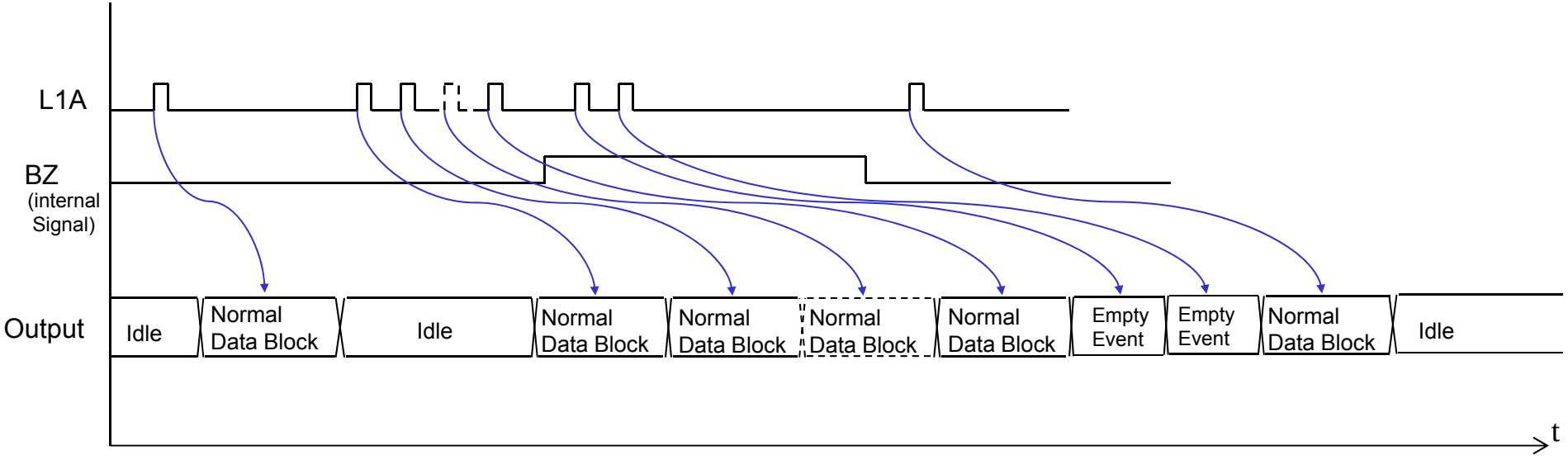
The BZ and OW flags are sent out on the next event-fragment to the DCC. Note that the flags are indicators of the HTR buffers, they are not related to the specific event-fragment where they are set.
When BZ=1, the HTR generates Empty-Events instead of regular events (this is a CMS requirement) .

Example of minimum L1A spacing that does not violates the Trigger rules



Example of DAQ-output sequence

In this example there are no rejected L1As (i.e. Trigger Rules are not violated)



Note that the BZ included in each Data Block, latches the value of the internal BZ at the beginning of each block transmission.

Address Section

Details on http://cmsdoc.cern.ch/cms/HCAL/document/CountingHouse/HTR/firmware/htr_vme.html

Total No of Local Bus Address Lines is 21.
Therefore Total Space : $2^{21} - 1$.
But addresses > 3FFF are indirectly accessd from VME due to pin shortage in the VME bridge. So better avoid them.