DCUF User Guide

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IMPORTANT NOTICE

Each DCUF contains a unique 24-bit Chip Identifier readable via I2C. DCUF is pin compatible with DCU2.

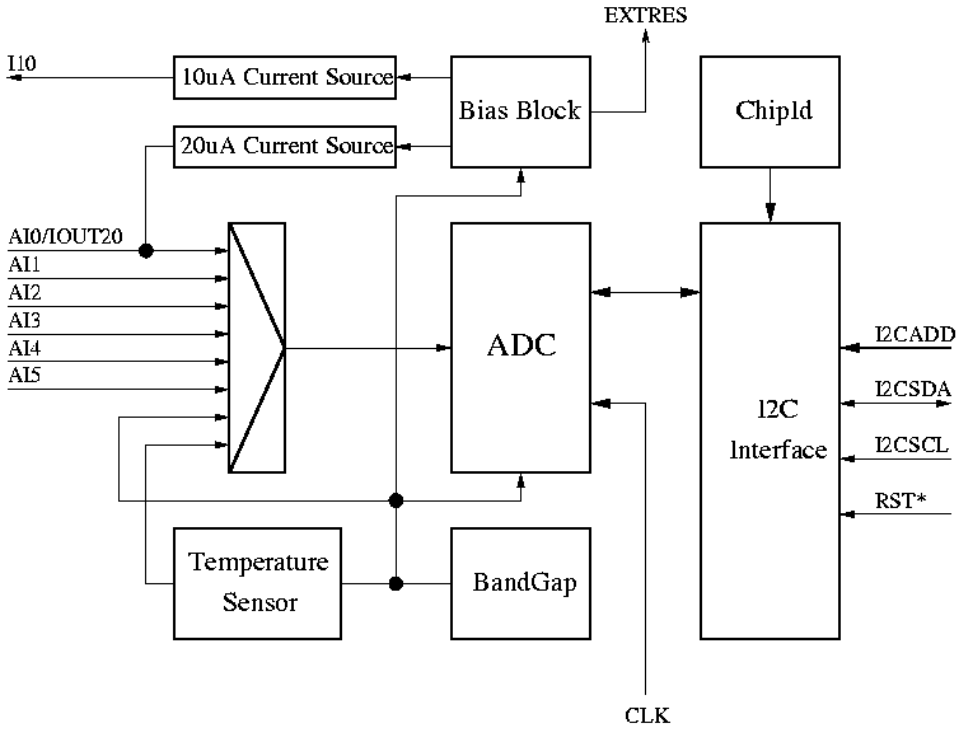
Introduction

This document is a simplified user manual for the first version of the integrated Detector Control Unit, a special ASIC to be used mainly in the CMS central tracker for the monitoring of some embedded parameters like supply voltage and currents on the front-end read-out modules.

This version of the ASIC is the final one, as from the specifications required by CMS

DCUF Architecture

The architecture of the DCUF is shown in the following block diagram.



The DCUF contains the following main blocks:

- a serial slave interface based on the standard I2C protocol,
- a band-gap voltage reference,
- an analogue multiplexer,

- a 10uA constant current source,
- a 12-bit ADC,
- one node controller (the CCU control itself is seen as a special channel capable for instance to report the status of the other CCU channels),
- an on-chip temperature sensor,
- a 20uA constant current source internally connected to one of the inputs of the analogue multiplexer,
- a set of fuses that fixes a unique 24-bit Chip Identifier.

The access to the internal registers of the DCUF is available though an I2C interface. The user can select one of the ADC input channels, start an ADC acquisition and read the ADC output or the 24-bit chip identifier simply by accessing different I2C registers.

A band-gap voltage reference gives to the ADC a stable reference voltage. An external voltage Vref can be applied to the DCUF instead of the one generated from the band-gap for test purposes only (not in the packaged version). The DCUF provides one 10 μA and one 20 μA current sources that can be used to drive external thermistors for temperature measurement.

Specifications

- Digital interface I/O: I2C Standard Protocol with 2.5 V CMOS levels
- Operating temperature range: -50°C -> +50°C
- Power consumption: < 40mW (VDD = 2.5V, T = 25°C $\Rightarrow$ I = 13 mA)
- Supply voltage: single VDD @ 2.5V
- Clock frequency: 40MHz
- Die size: 2x2mm
- No of pads: 27 (only 24 used in packaged version)
- Available in 24 pin LPCC package or as naked die

- Temperature Sensor Specifications

Gain	9.22 LSBs/°C	Resolution = 0.108 °C
Out @ 25°C	2469 (RMS = 32.28)	Calibration required
|INL|	< 2.5 LSBs	Evaluated in the range -30°C $\rightarrow$ +30°

- Temperature Sensor Specifications

Input Channels	7	only 6 available in packaged version, one – channel 0 – internally connected to the 20uA current source, one – channel 7 – internally connected to the integrated temperature sensor)
Input Range	~GND → VDD/2	LIR Mode
	VDD/2 → ~VDD	HIR Mode
Reference	GND	LIR Mode
	VDD	HIR Mode
Gain	2.22 LSBs	Resolution = 450 μV
Offset	< 2 LSBs	Offset < 1mV (Automatic oOffset cancellation)
|INL|	< 1 LSB	In the Input Range
|DNL|	< 1 LSB	Monotonic ADC, no missing codes
Noise RMS	< 0.5 LSB	Transition noise RMS
Conversion Time	0.25 msec	Maximum value
σ_T(Gain)	+120 ppm/°C	Evaluated in the range -30°C → +30°
σ_{VDD}(Gain)	-5 ppm/mV	Evaluated in the range 2.25V → 2.75V
σ_{Dose}(Gain)	-0.3%/MRad	Samples irradiated up to 10 MRad with X-Rays (rate = 25 Krad/min)

- 10uA current source specifications

I10uA	9.63 μA	
σ_T(I10uA)	-175 ppm/°C	Evaluated in the range -20°C → +80°
σ_{Dose}(I10uA)	+0.3%/MRad	Samples irradiated up to 10 MRad with X-Rays (rate = 25 Krad/min)

- 20uA current source specifications

I20uA	19.23 μA	
σ_T(I20uA)	-160 ppm/°C	Evaluated in the range -20°C → +80°
σ_{Dose}(I20uA)	+0.3%/MRad	Samples irradiated up to 10 MRad with X-Rays (rate = 25 Krad/min)

DCUF Internal Registers

Register Definitions

The DCUF contains the following 8-bit internal registers:

- Control Register (CREG)
- Auxiliary Register (AREG)
- Test Register (TREG)
- Status & Data High Register (SHREG)
- Data Low Register (LREG)
- Chip Identifier Low Register (IDLREG)
- Chip Identifier Medium Register (IDMREG)
- Chip Identifier High Register (IDHREG)

Three registers (CREG, AREG and TREG) are R/W; the remaining five (SHREG, LREG, IDLREG, IDMREG and IDHREG) are read only. The access to the 8 registers follows the I2C standard protocol. The 4 MSBs of the 7-bit I2C address are used to address the chip on an I2C bus; the remaining 3 bits are used to address the five internal registers according to the following table:

Register	I2C address <A2:A0>
CREG	000
SHREG	001
AREG	010
LREG	011
TREG	100
IDLREG	101
IDMREG	110
IDHREG	111

The full address of a register is therefore given by the concatenation of the high 4 externally settable addresses with the three internal register' address

As usual on an I2C bus, for both address and data the MSB is transmitted first.

Control Register (R/W)

The bit allocation of the Control Register is described below:

Bit(s)	Name	Function
7	START	"1" to start an A to D conversion
6	RESET	"1" to reset the r/w registers
5	HIRES	must be "0"
4	TSON	must be "0"
3	POLARITY	"1" in LIR Mode, "0" in HIR Mode
2:0	CHANNEL<2:0>	Selects the ADC input channel

Extended Control and Test Register (R/W)

Bit(s)	Name	Function
7	CNT_TEST	Used to test AD counter, must be written with 0
6	ADCFSM_TEST	Used to test AD control logic, must be written with 0
5	UNUSED	
4	BGON	Selects the bandgap reference, must be written with 1
3	FSMODE	Activates single scale mode, must be written with 0
2	DTPION	Stops AD counter on external trigger, must be written with 0
1	DTPO_SEL	Selects digital test point, must be written with 0
0	ATP_SEL	Selects analog test point, must be written with 0

This register is implemented mainly for test purposes and for normal operation must always be written with 0x10.

Auxiliary Register (R/W)

Bit(s)	Name	Function
7	AD_SET	Writes into results register, must be written with 0
6	AD_RESET	Writes into results register, must be written with 0
5	UNUSED	
4	UNUSED	
3:0	FSM_STATE	Used to test control logic of AD, must be written with 0

This register is implemented only for test purposes and must always be written with 0x00.

Status & Data High Register (R/W)

The bit allocation of the Status & Data High Register is here described:

Bit(s)	Function/internal signals
7	IDLE
6	SEU Error
5:4	UNUSED
3:0	DATA<11:8>

When IDLE is equal to "1" the DCU is in the IDLE state and a new acquisition can be started. The 4 MSBs of the result of the last ADC acquisition of the can be read in DATA.

Data Low Register (R/W)

The bit allocation of the Data Low Register is described below:

Bit(s)	Function/internal signals
7:0	DATA<7:0 >

The 8 LSBs of the result of the last ADC acquisition can be read in DATA.

Chip Identifier Low Register (read only)

The bit allocation of the Data Low Register is described below:

Bit(s)	Function/internal signals
7:0	CHIPIDL

The 8 LSBs CHIPID<7:0> of the Chip Identifier can be read in CHIPIDL.

Chip Identifier Medium Register (read only)

The bit allocation of the Data Low Register is described below:

Bit(s)	Function/internal signals
7:0	CHIPIDM

The 8 bits CHIPID<15:8> of the Chip Identifier can be read in CHIPIDM.

Chip Identifier High Register (read only)

The bit allocation of the Data Low Register is described below:

Bit(s)	Function/internal signals
7:0	CHIPIDH

The 8 MSBs CHIPID<23:16> of the Chip Identifier can be read in CHIPID.

DCUF Operations

HW Reset

A hardware reset of the DCUF R/W registers is performed forcing to "0" the RESET pin.

SW Reset

A software reset of the DCUF r/w registers is performed when a '1' is written into the bit 6 of the Control Register CREG (CREG<6>).

Acquire

An acquisition is started when a '1' is written into the bit 0 of the Control Register CREG (CREG<7>).

The bit CREG<2:0> selects the input channel according with the following table:

CREG<2:0>	ADC input channel
000	IA0
001	IA1
010	IA2
011	IA3
100	IA4
101	IA5
110	IA6
111	Temperature channel

Read Result

When the bit 0 of the Status & Data High Register SHREG<7> contains a '1', the DCUF is in the IDLE state and the result of the last ADC acquisition can be read:

- RES<11:8> = SHREG<3:0>
- RES<7:0> = LREG<7:0>

DCUF Conversion Operations

A conversion cycle of the ADC can simply be started by setting the proper channel address in the control register and setting the start conversion bit in the same register. The start conversion bit (START) is cleared automatically at the completion of the conversion. For instance, a conversion on the input channel 3 can be started by writing a "11011001" (i.e. 0xD9) into the Control register.

Read Chip Identifier

The 24-bit Chip Identifier can simply be accessed by reading in sequence the three registers IDHREG, IDMREG and IDLREG.

DCUF Pin Layout, Package and Pin Assignments

DCUF Pad Assignment

The DCUF die size is 2 x 2 mm; there are 27 normal pads with a 225um pitch and 3 extra corner pads for testing purposes only.

The pad position of the 31 pads in the die is represented in Fig.2.

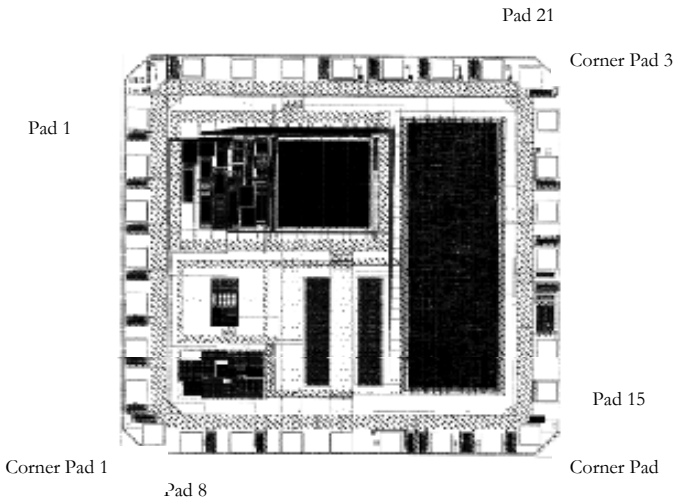


Fig.2: DCU pad position

Pad assignment

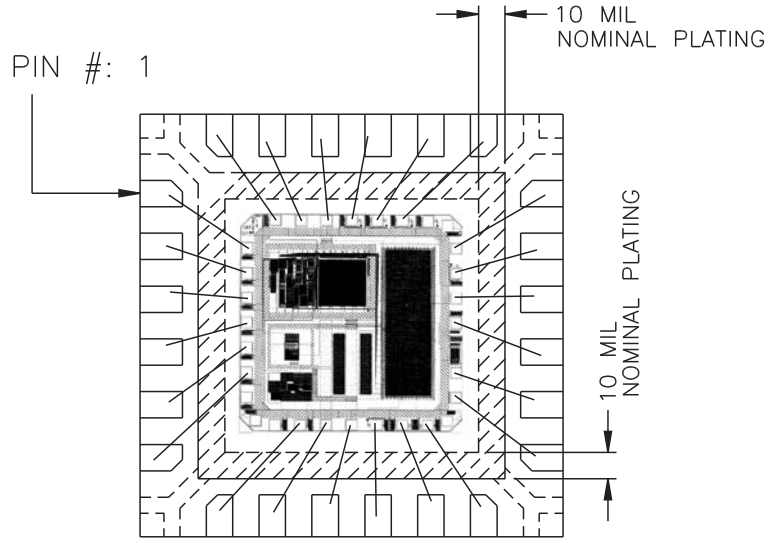
Pad assignement for DCUF

Pad	Signal	Comment
1	IA0/Iout20	
2	IA1	
3	IA2	
4	IA3	
5	IA4	
6	IA5	
7	IA6	
C1	Test1	Corner Pad 1
8	Vref	
9	ExtRes	
10	GND	
11	VDD	
12	I2CA3	

13	CLK-	
14	CLK+	
C2	Test2	Corner Pad 2
15	VDD	
16	I2CSDA	
17	I2CSCL	
18	GND	
19	ResetBar	
20	GND	
C3	Test3	Corner Pad 3
21	unused	
22	I2CA6	
23	I2CA5	
24	I2CA4	
25	VDD	
26	GND	
27	Iout10	

DCUF Packaged Version

The DCUF bonding in the LPCC24 package is given in the figure below:



CERN - DCU

E: 1) DOTTED LINE REFER TO HALF ETCH TIE BAR POSITION
2) RING PLATING L/F; HATCHING AREA IS REPRESENTED THE DAP BONDABLE AREA.

NG DIAGRAM DRAWING NO.:		REV.:	
REVIEWED BY FOL:		DWG REVIEWED BY MOLD:	
COUNT: 24L		LEAD FRAME MATERIAL: CU, C7025	
AGE DIMENSION: LPCC 4x4x0.9		LEAD FRAME THICKNESS: 8 MILS	
DMER:		MAXIMUM WIRE LENGTH:	
E:		GOLD WIRE DIAMETER:	
ZE (1):		DIE ATTACH MATERIAL:	
ZE (2):		MOLD COMPOUND:	
IZE: 110x110 MILS		DRAWN BY:	DATE:
DMER DOC. NO:	DATE:	REVIEWED BY:	DATE:
		UNIT:	DIE LOCATION:

Pin assignment in LPCC24

Pinout for DCU in LPCC24

1IA0/Iout20
2IA1
3IA2
4IA3
5IA4
6IA5
7ExtResistor
8GND
9VDD
10I2CA3
11CLK-
12CLK+
13VDD
14I2CSDA
15I2CSCL
16GND
17ResetBar
18GND
19I2CA6
20I2CA5
21I2CA4
22VDD
23GND
24Iout10

DCUF evaluation package

For evaluation purposes, the DCU has been packaged also in a 40-pin Dual-In-Line plastic package (DIP-40).