PLT Refurbishment Planning Document (USCMS)

April 2018

Due to continued radiation exposure the Run 2 PLT assembly is expected to become too degraded to be used after 2018. Hence, sensors and readout components will need replacement for the run period starting in 2021. This run period could continue until 2024. To provide spare parts for damage and prepare for degradation of the components with radiation we plan to acquire components for two PLT assemblies. While chips are available on two wafers from previous production at PSI (Danek) and one from FNAL (Marco), we are lacking readout boards. This document summarized the **readout boards** that need to be provided by USCMS to estimate the cost (and in this part serves as planning document).

System Overview

The readout components are, with the existing/required quantity listed in brackets

1. Hybrid Boards (12/96+)
2. HDI boards (5/32+)
3. Portcard Type 1a (8 bare, 5 equipped /4+)
4. Portcard Type 2 (4 bare, 4 equipped /4+)
5. Opto-Motherboard (8+)
6. AOH (3 fiber version/2 fiber version) (48+/12+)
7. DOH (10+)
8. Ribbon cable with connector (24+)
9. PPO (4+)

We have access to FED and FEC (mFEC) that became available from the Run 1 pixel detector – we have not yet secured them.

A readout test stand will be installed at Rutgers too be able to perform component testing.

A full readout chain is installed at CERN (P5 laboratory)

Details

1. Hybrid Boards (Fig. 1)

Components

- PSI46V2 readout chip (ROC)
- Sensor (n-on-n Si)
- Surface mount electronic components (~8)
- Wire for bias voltage

The board needs redesign to avoid solder shorts before submission. Design, specification, and submission by ED (Rutgers), review by Bert (Princeton). The existing 20 hybrids are at CERN.

At Rutgers surface components are mounted by technician.

At PSI the ROC will be mounted and the sensor bump bonded; wire bonding and initial testing. The assembly is then sent to CERN for further testing.

Alternatively, the wire bonding could happen at Rutgers – but at the cost of additional shipping.

Today there is agreement to manufacture 48 units; 20 units exist at CERN. Another 48 units will be needed to prepare a second version.

A single-plane test stand is installed at CERN. It is not established if single plane testing occurs at PSI; it is preferred. Preliminary planning is to provide a working test stand to PSI (missing components) to do testing before sending to CERN; iterate faulty components.

2. HDI Boards (Fig. 2)

Components

- TBM (token bit manager) TBM05a (2005) on wafer 2 PSI (~360)
- PLT driver chip
- Surface mount components
- Critical component: connectors as availability not yet established.

Board submission via Bert (Princeton).
At Rutgers, technician performs chip, component placement, wire bonding, and testing.
Component testing at CERN.

3. Port Card Type 1a

Cards available at CERN - 5 (require repair of chips)
Blank cards 8 at Rutgers

Components/board

- LCDS chip (4 or 5)
- Surface mount components
- Critical: connectors (correct gender)

Assembly at Rutgers; test if the 5th LCDS chip is still required.
Repair cards at CERN bonding lab;
equip and test at Rutgers (technician)

4. Port Card Type 2 (Fig. 3)
   Cards available at CERN 4 (require repair of chips) – probably repaired too often.
   Blank cards 4 at Rutgers
   We need to make 6 new blank boards and equip them.

Components/board

- LCDS chip (4 or 5)
- Surface mount components
- Critical: connectors (correct gender)

Repair cards at CERN bonding lab;
equip and test at Rutgers (technician)

5. Opto-Motherboard (OMB)

Components/board

- Slow hub chip (1)
- Slow hub adapter (1)
- Gatekeeper (1)
- Delay 25 (1)
- PLL chips (1)
- ALT chip (6)
- Surface mount components
- connectors

Four Opto-motherboards of the present version are available. There is no more supply of the slow hub chips. Furthermore, the gatekeeper chip is only available as die (not packaged). There is sufficient supply of a new version of the hub chip that combines slow hub and slow hub adapter (on wafer from FNAL; not diced).

The OMB requires redesign to include the new hub chip and the die gatekeeper chip. The design change is assessed by Ed to be uncritical. The testing of a prototype has high priority. In case problems with the new hub arise, chips can be probably added to a wafer submission from PSI (February). In this case the solution is either to submit a corrected version of the combined hub chip or fall back to the previous (proven) version. In the latter case, the board still needs to be adapted to the new gatekeeper chip.

Rutgers (Ed): test new chip with old OMB modified with hand-wiring it in – this tests the new hub chip (end of 2017). If successful, re-design the OMB board (Q1, Q2 2018); submission (Q3 2018 preferably by CERN or else via Bert (Princeton)); equipment, assembly by technician at Rutgers (Q4 2018).

A request to CERN for in-kind engineering support for the OMB should be made.

6./ 7. AOH / DOH

The DOHs are in critically short supply and these need to be carefully salvaged from the existing PLT detectors, taking care to remove the cover from the thermal paste with a thin blade. As a contingency harvesting the DOH's from the pixel phase-0 detector could be considered and will be investigated.

The present PLT and BCM1F use TEC 3 laser type AOHs. The inventory for the AOHs needs to be understood and tested. The use of 2 laser AOHs and 3 laser AOHs with the different connector (TOB vs TEC) could be explored for both PLT and BCM1F, and the layout of the OMB modified accordingly.

8. Flex cables

The flex cables should be ordered via the CERN PCB shop. The number of cables of required length and cost is to be clarified with Cathy.

Cost Estimate

The critical item is the design, testing, and production of 10 OMBs. The R&D phase requires 1 month engineering time to identify slow hub solutions, layout changes for the gate keeper chip and layout proposals for the AOH wiring (Ed) and another 2 weeks communicate the proposed engineering solution to CERN and resubmit all the boards (Bert, CERN).

The components that need order by USCMS are numbers 1., 2., 4..

The boards will be submitted via Bert with the old version design files, or new files obtained from Ed where changes were needed.

The manpower is 4 weeks engineering time (Ed), and 4 weeks of technician time.

The components to be requested to be order by CERN are 5.

Timeline

The work already started. Ed will work on the design end-of-year 2017, beginning of next year. This will allow participating in an ASIC submission with PSI in case the new hub chip fails.

The boards will be submitted asap and over the year 2018 all the components should be built and tested (will need extensive cold cycle testing as this is one of the failure modes we experienced).

One full working detector (forward/backward end) will be assembled in 2019 and subjected to further cold testing. The rebuilding of the mechanics/cooling structure is coordinated with CERN.

Item	**Cost**	**+ overhead**

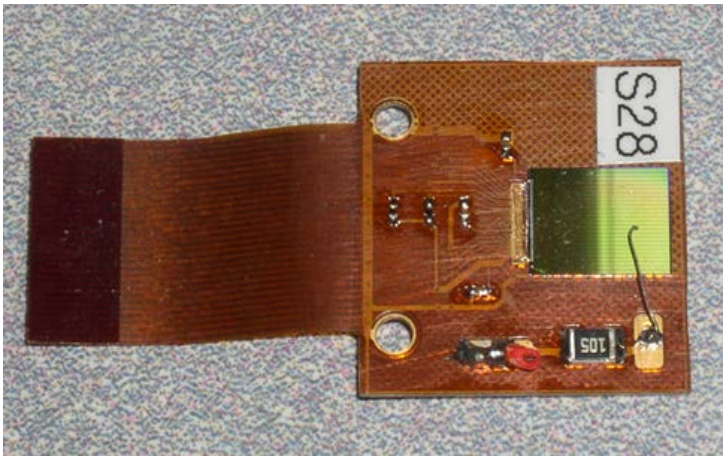

Figure 1: The hybrid board with the sensor.

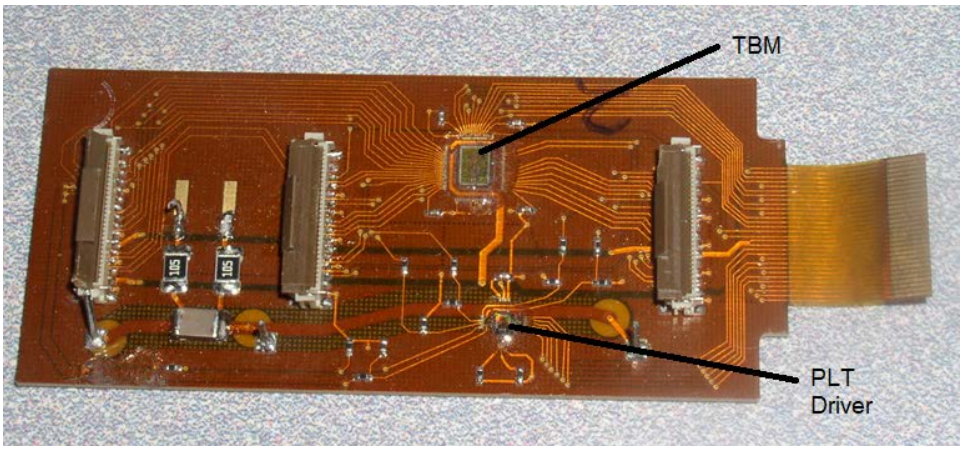

Figure 2: The HDI boards with connectors for 3 hybrid boards (component 2) corresponding to one telescope. The pig tail plugs into the port card – four HDI per portcard (PLT quarter).

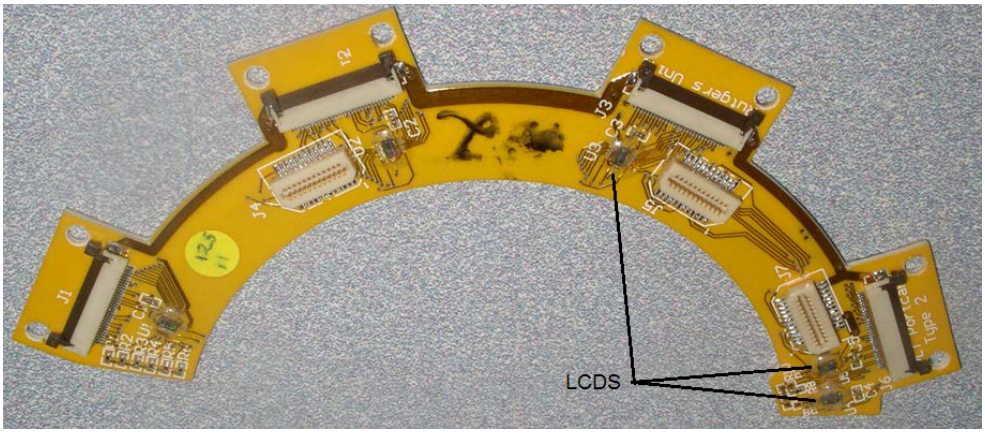

Figure 3: Port card (Type2) with connectors for four telescopes (outward)

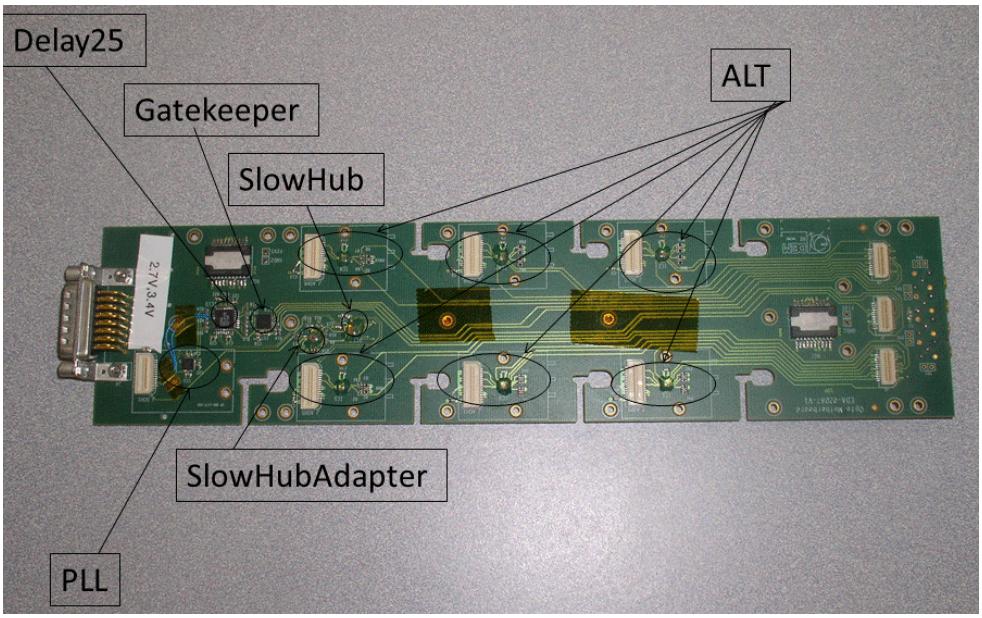

Figure 4: Opto-Motherboard (present version)