SKIROC2

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Abstract –

SKIROC (Silikon pin Kalorimeter Integrated ReadOut Chip) is the very front end chip designed for the readout of the Silicon PIN diodes foreseen for the Electromagnetic CALorimeter (ECAL) of the future International Linear Collider.

The very fine granularity of the ILC calorimeters implies a huge number of electronics channels (82 millions) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector without any external component making crucial the reduction of the power consumption to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).

SKIROC2 is a **64-channel front-end chip**, designed in AMS 0.35µm SiGe technology.

Each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator.

The measured charge is stored in a 15-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12-bit Wilkinson ADC.

Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level.

A bandgap ensures the stability versus supply voltage and temperature for all the requested reference in the analogue core.

The power consumption of each channel is about 1.5 mW/channel.

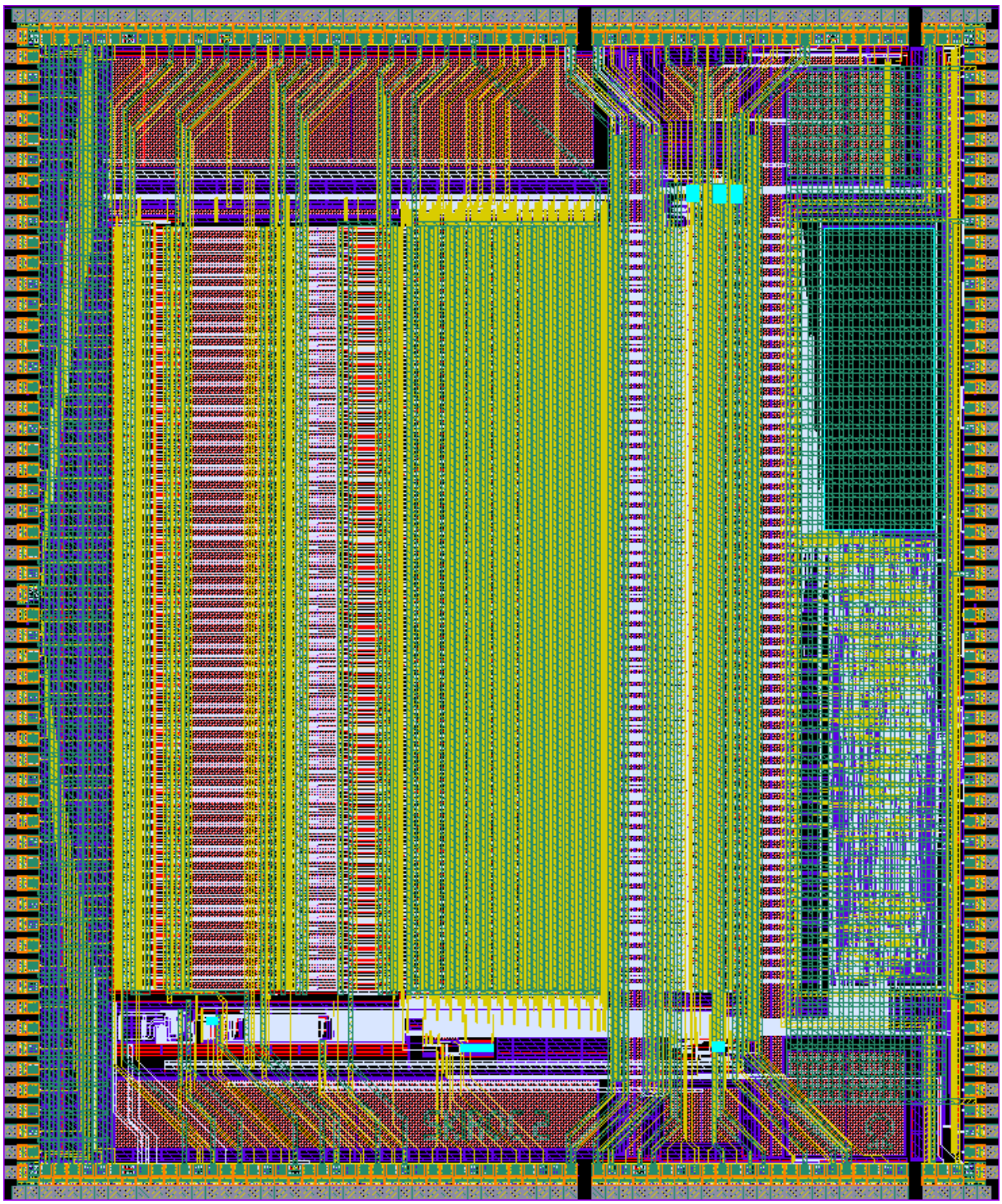

Figure 1 – SKIROC2 layout

- Technology: ***austriamicrosystems*** SiGe 0.35µm
- Die dimensions: 7.1 mm x 8.5 mm
- Package: QFP240 if packaged.

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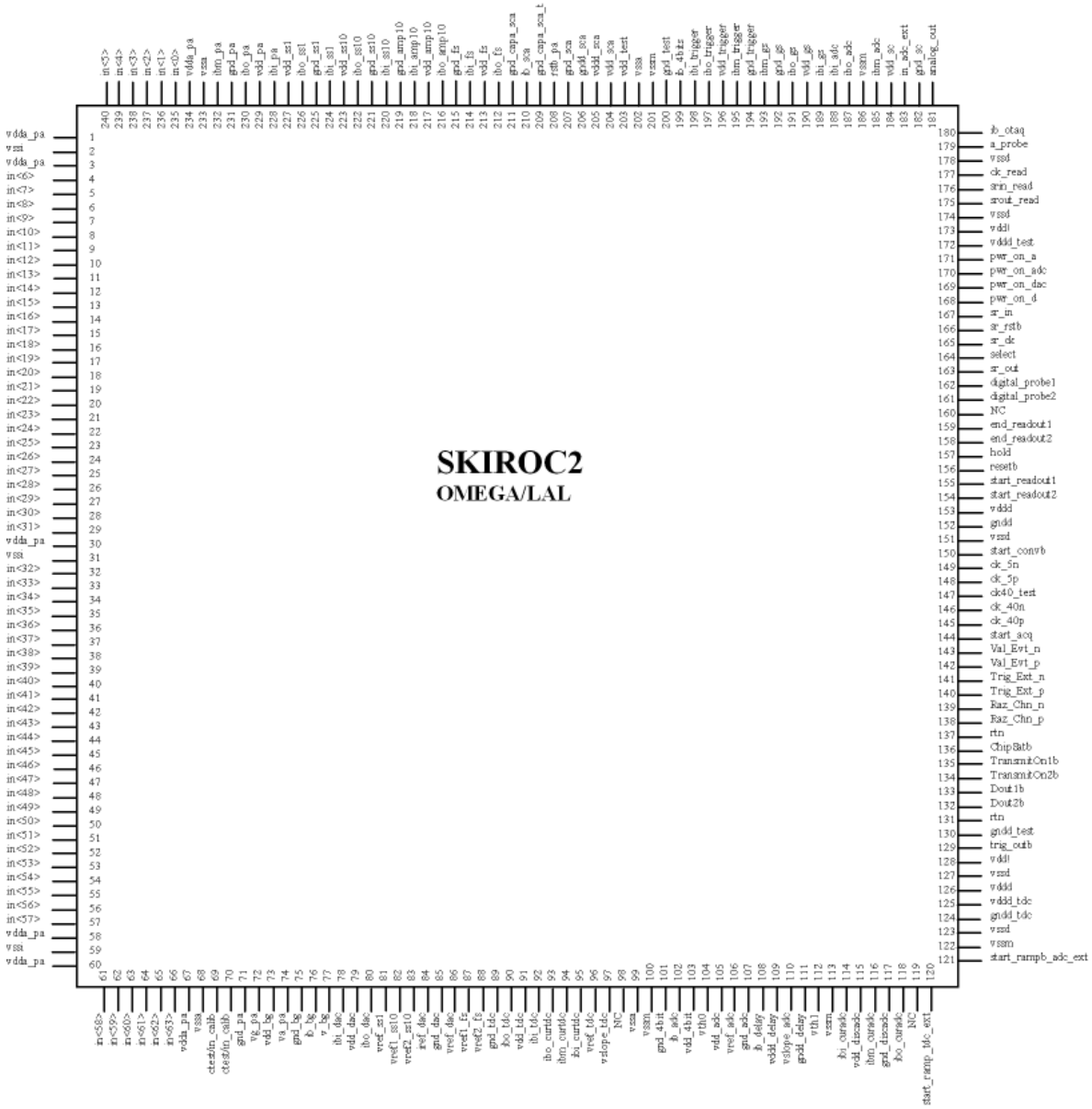


Figure 2 – SKIROC2 pinout

Pin	Pin Name	Pin Type	Description	Comments
1	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
2	vssi	Power	Inputs Bulk	to GND
3	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
4	in<6>	Analogue Input	Channel 6 to 31 inputs	
5	in<7>	Analogue Input	Channel 6 to 31 inputs	
6	in<8>	Analogue Input	Channel 6 to 31 inputs	
7	in<9>	Analogue Input	Channel 6 to 31 inputs	
8	in<10>	Analogue Input	Channel 6 to 31 inputs	
9	in<11>	Analogue Input	Channel 6 to 31 inputs	
10	in<12>	Analogue Input	Channel 6 to 31 inputs	
11	in<13>	Analogue Input	Channel 6 to 31 inputs	
12	in<14>	Analogue Input	Channel 6 to 31 inputs	
13	in<15>	Analogue Input	Channel 6 to 31 inputs	
14	in<16>	Analogue Input	Channel 6 to 31 inputs	
15	in<17>	Analogue Input	Channel 6 to 31 inputs	
16	in<18>	Analogue Input	Channel 6 to 31 inputs	
17	in<19>	Analogue Input	Channel 6 to 31 inputs	
18	in<20>	Analogue Input	Channel 6 to 31 inputs	
19	in<21>	Analogue Input	Channel 6 to 31 inputs	
20	in<22>	Analogue Input	Channel 6 to 31 inputs	
21	in<23>	Analogue Input	Channel 6 to 31 inputs	
22	in<24>	Analogue Input	Channel 6 to 31 inputs	
23	in<25>	Analogue Input	Channel 6 to 31 inputs	
24	in<26>	Analogue Input	Channel 6 to 31 inputs	
25	in<27>	Analogue Input	Channel 6 to 31 inputs	
26	in<28>	Analogue Input	Channel 6 to 31 inputs	
27	in<29>	Analogue Input	Channel 6 to 31 inputs	
28	in<30>	Analogue Input	Channel 6 to 31 inputs	
29	in<31>	Analogue Input	Channel 6 to 31 inputs	
30	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
31	vssi	Power	Inputs Bulk	to GND
32	in<32>	Analogue Input	Channel 32 to 57 inputs	
33	in<33>	Analogue Input	Channel 32 to 57 inputs	
34	in<34>	Analogue Input	Channel 32 to 57 inputs	
35	in<35>	Analogue Input	Channel 32 to 57 inputs	
36	in<36>	Analogue Input	Channel 32 to 57 inputs	
37	in<37>	Analogue Input	Channel 32 to 57 inputs	
38	in<38>	Analogue Input	Channel 32 to 57 inputs	
39	in<39>	Analogue Input	Channel 32 to 57 inputs	
40	in<40>	Analogue Input	Channel 32 to 57 inputs	
41	in<41>	Analogue Input	Channel 32 to 57 inputs	
42	in<42>	Analogue Input	Channel 32 to 57 inputs	
43	in<43>	Analogue Input	Channel 32 to 57 inputs	
44	in<44>	Analogue Input	Channel 32 to 57 inputs	
45	in<45>	Analogue Input	Channel 32 to 57 inputs	
46	in<46>	Analogue Input	Channel 32 to 57 inputs	

47	in<47>	Analogue Input	Channel 32 to 57 inputs	
48	in<48>	Analogue Input	Channel 32 to 57 inputs	
49	in<49>	Analogue Input	Channel 32 to 57 inputs	
50	in<50>	Analogue Input	Channel 32 to 57 inputs	
51	in<51>	Analogue Input	Channel 32 to 57 inputs	
52	in<52>	Analogue Input	Channel 32 to 57 inputs	
53	in<53>	Analogue Input	Channel 32 to 57 inputs	
54	in<54>	Analogue Input	Channel 32 to 57 inputs	
55	in<55>	Analogue Input	Channel 32 to 57 inputs	
56	in<56>	Analogue Input	Channel 32 to 57 inputs	
57	in<57>	Analogue Input	Channel 32 to 57 inputs	
58	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**
59	**vssi**	Power	Inputs Bulk	**to GND**
60	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**
61	in<58>	Analogue Input	Channel 58 to 63 inputs	
62	in<59>	Analogue Input	Channel 58 to 63 inputs	
63	in<60>	Analogue Input	Channel 58 to 63 inputs	
64	in<61>	Analogue Input	Channel 58 to 63 inputs	
65	in<62>	Analogue Input	Channel 58 to 63 inputs	
66	in<63>	Analogue Input	Channel 58 to 63 inputs	
67	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**
68	**vssa**	Power	Analogue part Bulk	**to GND**
69	c_test / in_calib	Analogue Input	Calibration input	
70	c_test / in_calib	Analogue Input	Calibration input	
71	**gnd_pa**	Power	Analogue (PreAmplifier) Ground	**to GND**
72	vg_pa	Analogue Bias	PreAmps bias voltage	
73	**vdd_bg**	Power	Analogue (BandGap) Power Supply	**to 3.3V**
74	va_pa	Analogue Bias	PreAmps bias voltage	
75	**gnd_bg**	Power	Analogue (BandGap) Ground	**to GND**
76	ib_bg	Analogue Bias	BandGap OTA bias current	
77	v_bg	Analogue Output	BandGap output	
78	ibi_dac	Analogue Bias	10-bit dual DAC OTAs Input stage bias	
79	**vdd_dac**	Power	Analogue (10-bit dual DAC) Power Supply	**to 3.3V**
80	ibo_dac	Analogue Bias	10-bit dual DAC OTAs Output stage bias	
81	vref_ss1	Analogue Bias	Gain1 Slow Shapers bias voltage	
82	vref1_ss10	Analogue Bias	Gain10 Slow Shapers bias1 voltage	
83	vref2_ss10	Analogue Bias	Gain10 Slow Shapers bias2 voltage	
84	iref_dac	Analogue Bias	10-bit dual DAC bias current	
85	**gnd_dac**	Power	Analogue (10-bit dual DAC) Ground	**to GND**
86	vref_dac	Analogue Bias	10-bit dual DAC OTAs bias voltage	
87	vref1_fs	Analogue Bias	Fast Shapers bias1 voltage	
88	vref2_fs	Analogue Bias	Fast Shapers bias2 voltage	
89	**gnd_tdc**	Power	Analogue (Time to Digital Convertor) Ground	**to GND**
90	ibo_tdc	Analogue Bias	TDC ramp integrator output stage bias current	

91	**vdd_tdc**	Power	Analogue (Time to Digital Convertor) Power Supply	**to 3.3V**
92	ibi_tdc	Analogue Bias	TDC ramp integrator input stage bias current	
93	ibo_curtdc	Analogue Bias	TDC ramp current source output stage bias current	
94	ibm_curtdc	Analogue Bias	TDC ramp current source middle stage bias current	
95	ibi_curtdc	Analogue Bias	TDC ramp current source input stage bias current	
96	vref_tdc	Analogue Bias	TDC ramp reference bias voltage	
97	vslope_tdc	Analogue Bias	TDC ramp slope bias voltage	
98	***NC***			
99	**vssa**	Power	Analogue part Bulk	**to GND**
100	**vssm**	Power	Mixed part Bulk	**to GND**
101	**gnd_4bit**	Power	Mixed (4-bit DAC adjustment) Ground	**to GND**
102	ib_adc	Analogue Bias	ADC ramp integrator bias current	
103	**vdd_4bit**	Power	Mixed (4-bit DAC adjustment) Power Supply	**to 3.3V**
104	vth0	Analogue Output	10-bit dual DAC output0 (Trigger Discriminator Threshold)	
105	**vdd_adc**	Power	Mixed (ADC Discriminator) Power Supply	**to 3.3V**
106	vref_adc	Analogue Bias	ADC ramp reference bias voltage	
107	**gnd_adc**	Power	Mixed (ADC Discriminator) Ground	**to GND**
108	ib_delay	Analogue Bias	Trigger delay cell bias current	
109	**vddd_delay**	Power	Digital (Trigger Delay) Power Supply	**to 3.3V**
110	vslope_adc	Analogue Bias	ADC ramp slope bias voltage	
111	**gndd_delay**	Power	Digital (Trigger Delay) Ground	**to GND**
112	vth1	Analogue Output	10-bit dual DAC output1 (Gain Selection Discriminator Threshold)	
113	**vssm**	Power	Mixed part Bulk	**to GND**
114	ibi_curadc	Analogue Bias	ADC ramp current source input stage bias current	
115	**vdd_discadc**	Power	Mixed (ADC Discriminator) Power Supply	**to 3.3V**
116	ibm_curadc	Analogue Bias	ADC ramp current source middle stage bias current	
117	**gnd_discadc**	Power	Mixed (ADC Discriminator) Ground	**to GND**
118	ibo_curadc	Analogue Bias	ADC ramp current source output stage bias current	
119	***NC***			
120	start_ramp_tdc_ext	Digital Input	External TDC Ramp Start Signal	Active H
121	start_rampb_adc_ext	Digital Input	External ADC Ramp Start Signal	Active L
122	**vssm**	Power	Mixed part Bulk	**to GND**
123	**vssd**	Power	Digital part Bulk	**to GND**
124	**gndd_tdc**	Power	Digital (TDC ramp control) Ground	**to GND**
125	**vddd_tdc**	Power	Digital (TDC ramp control) Power Supply	**to 3.3V**
126	**vddd**	Power	Digital (POD, LVDS receivers & digital glue) Power Supply	**to 3.3V**
127	**vssd**	Power	Digital part Bulk	**to GND**
128	**vdd!**	Power	Digital (Digital ASIC) Power Supply	**to 3.3V**

129	trig_outb	Digital Output	OR of the 64 triggers	Active L / weak OC
130	**gndd_test**	Power	Test purpose Digital Ground	**to GND**
131	rtn	Power	Open Collector Ground	**to GND**
132	Dout2b	Digital OC Output	Data Serial Output	Open Collector
133	Dout1b	Digital OC Output	Data Serial Output	Open Collector
test	Dout (test)	Digital OC Output	Data Serial Output	Open Collector
134	TransmitOn2b	Digital OC Output	Active data readout	Open Collector / Active H
135	TransmitOn1b	Digital OC Output	Active data readout	Open Collector / Active H
136	ChipSatb	Digital OC Output	Analogue memory full / => Acq stopped	Open Collector / Active H
test	TransmitOn (test)	Digital OC Output	Active data readout	Open Collector / Active H
137	rtn	Power	Open Collector Ground	**to GND**
138	Raz_Chn_p	Digital (LVDS) Input	Erase active Analogue Column.	Active H
139	Raz_Chn_n			
140	Trig_Ext_p	Digital (LVDS) Input	External Trigger input	Active ↑
141	Trig_Ext_n			
142	Val_Evt_p	Digital (LVDS) Input	Disable discriminator output signal	Active L
143	Val_Evt_n			
test	start_acq (test)	Digital Input	Test purpose Start acquisition on analogue memory	Active H
144	start_acq	Digital Input	Start & allow acquisition on analogue memory	Active H
145	CK_40p	Digital (LVDS) Input	40MHz Clock	
146	CK_40n			
147	ck40_test	Digital Input	Test purpose : 40MHz single input	
148	CK_5p	Digital (LVDS) Input	Slow Clock (Acquisition = 5MHz , ReadOut = 1MHz)	
149	CK_5n			
150	start_convb	Digital Input	Start conversion signal	Active L
test	start_convb (test)	Digital Input	Test purpose Start conversion signal	Active L
151	**vssd**	Power	Digital part Bulk	**to GND**
152	**gndd**	Power	Digital (POD, LVDS receivers & digital glue) Ground	**to GND**
153	**vddd**	Power	Digital (POD, LVDS receivers & digital glue) Power Supply	**to 3.3V**
test	start_readout (test)	Digital Input	Test purpose Digital RAM start readout signal	Active H
154	start_readout2	Digital Input	Digital RAM start readout signal	Active H
155	start_readout1	Digital Input	Digital RAM start readout signal	Active H
156	resetb	Digital Input	Reset ASIC digital part	Active L
test	resetb (test)	Digital Input	Test purpose Reset ASIC digital part	Active L
157	hold	Digital Input	Backup Analogue Memory Hold Signal	Active H
158	end_readout2	Digital Output	Digital RAM end readout signal	Active H
159	end_readout1	Digital Output	Digital RAM end readout signal	Active H

test	end_readout (test)	Digital Output	Test purpose Digital RAM end readout signal	Active H
160	***NC***			
161	digital_probe2	Digital Output	Digital Probe 2 Output	
162	digital_probe1	Digital Output	Digital Probe 1 Output	
test	sr_out (test)	Digital Output	Test purpose Selected Register Output	
163	sr_out	Digital Output	Selected Register Output	
164	select	Digital Input	Select Slow Control Register (1) or Probe Register (0)	
165	sr_ck	Digital Input	Selected Register Clock	Active ↑
test	sr_ck (test)	Digital Input	Test purpose Selected Register Clock	Active ↑
166	sr_rstb	Digital Input	Selected Register Reset	Active L
167	sr_in	Digital Input	Selected Register Input	
168	pwr_on_d	Digital Input	Digital Power Pulsing Control	Active H
test	sr_in (test)	Digital Input	Test purpose Selected Register Input	
169	pwr_on_dac	Digital Input	DAC Power Pulsing Control	Active H
170	pwr_on_adc	Digital Input	ADC Power Pulsing Control	Active H
171	pwr_on_a	Digital Input	Analogue Part Power Pulsing Control	Active H
172	**vddd_test**	Power	Test purpose Power Supply	NC
173	**vdd!**	Power	Digital (Digital ASIC) Power Supply	**to 3.3V**
174	**vssd**	Power	Digital part Bulk	**to GND**
175	srout_read	Digital Output	Read Register Output	
176	srin_read	Digital Input	Read Register Input	
177	ck_read	Digital Input	Read Register Clock	
178	**vssd**	Power	Digital part Bulk	**to GND**
179	a_probe	Analogue Output	Analogue Probe Output	
180	ib_otaq	Analogue Bias	Analogue outputs OTA bias	
181	analog_out	Analogue Output	Multiplexed SCA Analogue Output	
182	**gnd_sc**	Power	Digital (Slow Control Register) Ground	**to GND**
183	in_adc_ext	Analogue Input	ADC External input	
184	**vdd_sc**	Power	Digital (Slow Control Register) Power Supply	**to 3.3V**
185	ibm_adc	Analogue Bias	ADC discriminator middle stage bias current	
186	**vssm**	Power	Mixed part Bulk	**to GND**
187	ibo_adc	Analogue Bias	ADC discriminator output stage bias current	
188	ibi_adc	Analogue Bias	ADC discriminator input stage bias current	
189	ibi_gs	Analogue Bias	Gain Selector input stage bias current	
190	**vdd_gs**	Power	Mixed (Gain Selection, Analog Trigger Delay, OTAq) Power Supply	**to 3.3V**
191	ibo_gs	Analogue Bias	Gain Selector output stage bias current	
192	**gnd_gs**	Power	Mixed (Gain Selection, Analog Trigger Delay, OTAq) Ground	**to GND**
193	ibm_gs	Analogue Bias	Gain Selector middle stage bias current	
194	**gnd_trigger**	Power	Mixed (Trigger discriminator) Ground	**to GND**
195	ibm_trigger	Analogue Bias	Trigger discriminator middle stage bias current	

196	**vdd_trigger**	Power	Mixed (Trigger discriminator) Power Supply	**to 3.3V**
197	ibo_trigger	Analogue Bias	Trigger discriminator output stage bias current	
198	ibi_trigger	Analogue Bias	Trigger discriminator input stage bias current	
199	ib_4bits	Analogue Bias	4-bit DAC adjustement stage bias current	
200	**gnd_test**	Power	Test purpose Ground	**to GND**
201	**vssm**	Power	Mixed part Bulk	**to GND**
202	**vssa**	Power	Analogue part Bulk	**to GND**
203	**vdd_test**	Power	Test purpose Power Supply	NC
204	**vdd_sca**	Power	Analogue (Switched Capacitor Array) Power Supply	**to 3.3V**
205	**vddd_sca**	Power	Digital (Switched Capacitor Array) Power Supply	**to 3.3V**
206	**gndd_sca**	Power	Digital (Switched Capacitor Array) Ground	**to GND**
207	**gnd_sca**	Power	Analogue (Switched Capacitor Array) Ground	**to GND**
208	rstb_pa	Digital Input	Charge PreAmp Reset Signal	Active L
209	**gnd_capa_sca_t**	Power	Analogue (Time SCA) Ground	**to GND**
210	ib_sca	Analogue Bias	SCA bias current	
211	**gnd_capa_sca**	Power	Analogue (Charge SCA) Ground	**to GND**
212	ibo_fs	Analogue Bias	Fast Shaper output stage bias	
213	**vdd_fs**	Power	Analogue (Fast Shaper) Power Supply	**to 3.3V**
214	ibi_fs	Analogue Bias	Fast Shaper input stage bias	
215	**gnd_fs**	Power	Analogue (Fast Shaper) Ground	**to GND**
216	ibo_amp10	Analogue Bias	Gain10 Amplifier output stage bias current	
217	**vdd_amp10**	Power	Analogue (Amplifier Gain 10) Power Supply	**to 3.3V**
218	ibi_amp10	Analogue Bias	Gain10 Amplifier input stage bias current	
219	**gnd_amp10**	Power	Analogue (Amplifier Gain 10) Ground	**to GND**
220	ibi_ss10	Analogue Bias	Gain10 Slow Shaper input stage bias current	
221	**gnd_ss10**	Power	Analogue (Slow Shaper Gain 10) Ground	**to GND**
222	ibo_ss10	Analogue Bias	Gain10 Slow Shaper output stage bias current	
223	**vdd_ss10**	Power	Analogue (Slow Shaper Gain 10) Power Supply	**to 3.3V**
224	ibi_ss1	Analogue Bias	Gain1 Slow Shaper input stage bias current	
225	**gnd_ss1**	Power	Analogue (Slow Shaper Gain 1) Ground	**to GND**
226	ibo_ss1	Analogue Bias	Gain1 Slow Shaper output stage bias current	
227	**vdd_ss1**	Power	Analogue (Slow Shaper Gain 1) Power Supply	**to 3.3V**
228	ibi_pa	Analogue Bias	PreAmps input stage bias current	

229	**vdd_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**
230	ibo_pa	Analogue Bias	PreAmps output stage bias current	
231	**gnd_pa**	Power	Analogue (PreAmplifier) Ground	**to GND**
232	ibm_pa	Analogue Bias	PreAmps middle stage bias current	
233	**vssa**	Power	Analogue part Bulk	**to GND**
234	**vdda_pa**	Power	Analogue (PreAmplifier) Power Supply	**to 3.3V**
235	in<0>	Analogue Input	Channel 0 to 5 inputs	
236	in<1>	Analogue Input	Channel 0 to 5 inputs	
237	in<2>	Analogue Input	Channel 0 to 5 inputs	
238	in<3>	Analogue Input	Channel 0 to 5 inputs	
239	in<4>	Analogue Input	Channel 0 to 5 inputs	
240	in<5>	Analogue Input	Channel 0 to 5 inputs	

Table 1 - Pinout description

4. General description

The analog part (Figure 3) has been designed to handle a dynamic range from 0.1 MIP (1Mip=4 fC) up to 2500 MIPs. The detector capacitance has been estimated to 20pF taking account the 25mm^2 pin diode and the PCB.

Each of the 64 channels is made on an input charge preamplifier. A common gain can be set by changing the feedback capacitor *Cf* using the Slow Control parameters. Each preamplifier is followed by a slow channel for the charge measurement and by a fast channel for trigger generation.

The fast channel is made of a high gain variable CRRC shaper (t*p* tunable between 50 ns and 100 ns thanks to the SC parameters) and is followed by a low offset discriminator to auto trig down to 0.1 MIP. The threshold of the 64 discriminators is supplied by a common 10-bit DAC and a 4-bit DAC per channel for each discriminator. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns using the SC parameters) to provide the Hold signal for the slow channel. A wired OR of the 64 triggers is available on pin 120 (trig_outb).

The slow channel is made of a low gain and high gain CRRC shapers to handle the large dynamic range. Each one is followed by a Track and Hold. As soon as there is an HOLD signal, the charge is stored in a 15 depth SCA as well as the time of each event (time tagging is performed thanks to a 12-bit TDC ramp).

The time and charges stored in the SCA cells are then converted by a 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory.

The power consumption has been optimized to reach an ultra low consumption: about 1.5 mW/channel. This chip can be power pulsed. Each stage can be individually shut down when not used.

Many configurations are available and are set using a slow control registers detailed in Table 2.

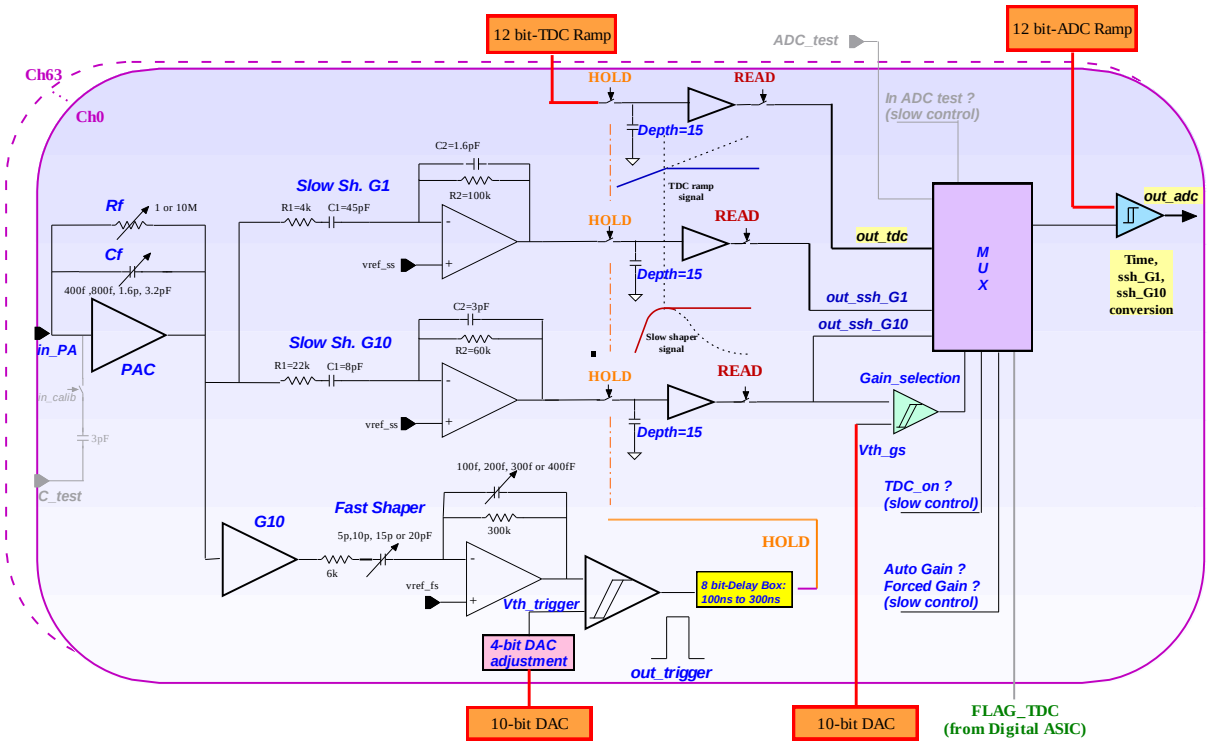


Figure 3 – SKIROC2: analog part simplified scheme

Register Name	bits	Register description	Subadd	Default Value
EN_PA	1	Enable preamplifiers	0	1 (PA Enabled)
PP: PreAmplifier	1	DisablePreAmp power pulsing mode (force ON)	1	0 (power pulsing mode)
GC : Capacitor PA Comp	3	PreAmp compensation capacitances commands (2…0)	2	111
GC : Capacitor PA Fdbck	4	PreAmp feedback capacitances commands (3…0)	5	1111
PA : PreAmp, In_calib & I_leakage	192	Disable charge preamp + Enable calibration capacitor + Select High Leakage Current Channel (from channel 0 to 63)	9	64 x 000 (All PA on, no Ctest, weak leakage)
EN_Slow Shaper Gain 1	1	Enable Slow Shaper G1	201	1 (SS_G1 Enabled)
PP: Slow Shaper Gain 1	1	Disable Slow Shaper G1 power pulsing mode (force ON)	202	0 (power pulsing mode)
EN_Slow Shaper Gain 10	1	Enable Slow Shaper G10	203	1 (SS_G10 Enabled)
PP: Slow Shaper Gain 10	1	Disable Slow Shaper G10 power pulsing mode (force ON)	204	0 (power pulsing mode)
EN_Fast Shaper	1	Enable fast shaper	205	1 (FSb Enabled)
PP: Fast Shaper	1	Disable fast shaper power pulsing mode (force ON)	206	0 (power pulsing mode)
GC : Time Constant Fast Shaper	2	Fast Shaper time constant commands (1…0)	207	00
EN_SCA	1	Enable SCA	209	1 (SCA Enabled)
PP: SCA	1	Disable SCA power pulsing mode (force ON)	210	0 (power pulsing mode)
GC : Backup SCA selection	1	Backup SCA selection (15-depth SCA = 0 , backup SCA = 1)	211	0 (15 depth SCA)
EN_SCA_backup	1	Enable backup SCA	212	1 (SCA Enabled)
PP: SCA_backup	1	Disable backup SCA power pulsing mode (force ON)	213	0 (power pulsing mode)
GC : SCA bias (Widlar)	1	Track & Hold/SCA bias (weak bias = 0 , high bias = 1)	214	0 (weak bias)
EN_Output OTAq	1	Enable Hi-Z Output OTA	215	1 (Output OTA Enabled)
PP: Output OTAq	1	Disable Hi-Z Output OTA power pulsing mode (force ON)	216	0 (power pulsing mode)
EN_Probe OTAq	1	Enable Probe OTA	217	1 (Probe Enabled)
PP: Probe OTAq	1	Disable Probe OTA power pulsing mode (force ON)	218	0 (power pulsing mode)
EN_DAC_4bit	1	Enable 4-bit DAC Adjustment	219	1 (Adjustment Enabled)
PP: DAC_4bit	1	Disable 4-bit DAC Adjustment power pulsing mode (force ON)	220	0 (power pulsing mode)
EN_Trigger	1	Enable Trigger Discriminator	221	1 (Trigger Enabled)
PP: Trigger Discri	1	Disable Trigger Discriminator power pulsing mode (force ON)	222	0 (power pulsing mode)
DA : 4-bit DAC Threshold Adjustment	256	Discri 4-bit DAC – from channel 0 to 63 (from LSB to MSB)	223	0001 (# 8)
TM : Trigger Mask	64	Allows to Mask Trigger (channel 63 to 0)	479	64 x 0 (no mask)
EN_Delay_Trigger	1	Enable Trigger delay function	543	1 (Trigger Delay Enabled)

PP: **Delay_Trigger**	1	Disable Trigger delay power pulsing mode (force ON)	544	0 (power pulsing mode)
GC : **Delay_Trigger**	8	Delay for the ”trigger” signals (From MSB to LSB)	545	0111 0000 (# 70)
GC : **Auto Gain**	1	Auto gain selection	553	1 (Auto Gain)
GC : **Forced Gain**	1	Chooses the gain value when auto gain selection is OFF (HG = 0 , LG = 1)	554	0 (High Gain)
GC : **Bypass Latch GS**	1	Enable LVDS receivers	555	0 (LVDS rec Disabled)
EC : **Sel In ADC Ext**	1	Select In_ADC_Ext as analogue data to convert (for ADC caracterisation)	556	0 (OFF)
PP: **Gain Select Discri**	1	Disable Gain Select Discriminator power pulsing mode (force ON)	557	0 (power pulsing mode)
EN_Gain_Select	1	Enable Gain Select Discriminator	558	1 (GS Discri Enabled)
EN_ADC_Discri	1	Enable ADC Discriminator	559	1 (ADC Discri Enabled)
PP: **ADC Discri**	1	Disable ADC Discriminator power pulsing mode (force ON)	560	0 (power pulsing mode)
EN_Bandgap	1	Enable Bandgap OTA	561	1 (Bandgap OTA Disabled)
PP: **Bandgap**	1	Disable Bandgap OTA power pulsing mode (force ON)	562	0 (power pulsing mode)
EN_10-bit Dual DAC	1	Enable 10-bit dual DAC	563	1 (DACs Enabled)
PP: **10-bit Dual DAC**	1	Disable 10-bit Dual DAC power pulsing mode (force ON)	564	0 (power pulsing mode)
GC : **DAC0 : Trigger**	10	10-bit DAC (From MSB to LSB) for Trigger Discriminator Threshold	565	11 1111 1111 (# 3FF)
GC : **DAC1 : Gain Select**	10	10-bit DAC (From MSB to LSB) for Gain Select Discriminator Threshold	575	11 1111 1111 (# 3FF)
EN_TDC_Ramp	1	Enable TDC Ramp	585	1 (TDC Ramp Enabled)
PP: **TDC Ramp**	1	Disable TDC Ramp power pulsing mode (force ON)	586	0 (power pulsing mode)
GC : **Comp_TDC_Ramp**	1	Enable TDC Ramp switch injected charge compensation	587	0 (No compensation)
GC : **TDC Ramp Slope**	1	TDC ramp slope (ILC : 200ns = 1, TestBeam : 5us = 0)	588	1 (200ns)
EN_ADC_Ramp	1	Enable ADC Ramp	589	1 (ADC Ramp Enabled)
PP: **ADC Ramp**	1	Disable ADC Ramp power pulsing mode (force ON)	590	0 (power pulsing mode)
EC : **Sel StartRampADC Ext**	1	Select External ADC Ramp commands (for ADC Ramp caracterisation)	591	0 (use ASIC commands)
GC : **Comp_ADC_Ramp**	1	Enable ADC Ramp switch injected charge compensation	592	0 (No compensation)
GC : **ADC Ramp Slope**	1	ADC ramp slope (10 bits = 1, 12 bits = 0)	593	0 (12 bits)
GC : **TDC On**	1	Allow use of TDC	594	1 (TDC On)
EC : **Sel Flag TDC Ext**	1	Select External Flag_TDC commands	595	0 (use ASIC commands)
GC : **Forced Flag_TDC**	1	Select analogue signal to digitize when Flag_TDC_External selected	596	0
EC : **Sel StartRampTDC Ext**	1	Select External TDC Ramp commands (for TDC Ramp caracterisation)	597	0 (use ASIC commands)

GC : Chip ID (8 bits)	8	Chip ID (from LSB to MSB)	598	1111 1111 (# FF)
EC : Sel Trig_Ext	1	Select only external Triggers as sampling command	606	1 (only Trig Ext)
EC : EN Trig Out	1	Enable weak Open Collector Trigger Out signal	607	1 (Trig Out Enabled)
PP: LVDS rec	1	Disable LVDS receivers power pulsing mode (force ON)	608	1 (LVDS rec ON)
EC : End_ReadOut	1	Enable End_ReadOut1 ('1') or End_ReadOut2 ('0')	609	1 (End_ReadOut1)
EC : Start_ReadOut	1	Select Start_ReadOut1 ('1') or Start_ReadOut2 ('0')	610	1 (Start_ReadOut1)
EC : ChipSat	1	Enable Opened collector ChipSat signal	611	1 (ChipSat Enabled)
EC : TransmitOn2	1	Enable Opened collector TransmitOn2 signal	612	1 (TransmitOn2 Enabled)
EC : TransmitOn1	1	Enable Opened collector TransmitOn1 signal	613	1 (TransmitOn1 Enabled)
EC : Dout2	1	Enable Opened collector Dout2 signal	614	1 (Dout2 Enabled)
EC : Dout1	1	Enable Opened collector Dout1 signal	615	1 (Dout1 Enabled)
Total	**616**		616	

PP : Power Pulsing
GC : General Configuration
EC : External Communication
TM : Trigger Mask
PA : PreAmplifier
DA : 4-bit DAC Adjustment

Table 2 – Slow Control parameters

Signal name	Probe	Comments	Probe output	Subadd
Out_SS1 / Out_SS10 / Out_PA	192	From channel 0 to 63	Analogue probe	0
Holdb_SCA	960	(Note: From channel 0 to 63 for even columns) (Note: From channel 63 to 0 for odd columns) From Column 0 to column 14	Digital probe 2	192
Threshold / Out_fsb	128	From channel 0 to 63	Analogue probe	1152
Out_t / Out_t_delayed	128	From channel 63 to 0	Digital probe 1	1280
Out_Gain / Out_ADC	128	From channel 0 to 63	Digital probe 2	1408
OR64 / OR64_delayed	2		Digital probe 1	1536
Start_ramp_TDC	1		Digital probe 2	1538
Start_ramp_TDC_Dig	1		Digital probe 2	1539
Flag_TDC	1		Digital probe 2	1540
Startb_ramp_ADC_Int	1		Digital probe 2	1541
Out_ramp_ADC	1		Analogue probe	1542
Out_ramp_TDC	1		Analogue probe	1543
Total	**1544**			1544

Table 3 – Probe register

Slow Control : ADC Ext Input	Slow Control : TDC On	***Flag TDC***	Slow Control : Auto Gain	Slow Control : Forced Gain	***ANALOG OUTPUT***
0	**0**	**0**	**X**	**X**	**High Gain**
0	**0**	**1**	**X**	**X**	**Low Gain**
0	**1**	**0**	**X**	**X**	**TDC Ramp**
0	**1**	**1**	**0**	**0**	**High Gain**
0	**1**	**1**	**0**	**1**	**Low Gain**
0	**1**	**1**	**1**	**X**	**Gain**: depends on GainSelect Discriminator
1	**X**	**X**	**X**	**X**	**ADC Ext Input**
ON (1) / OFF (0)	ON (1) / OFF (0)		ON (1) / OFF (0)	HIGH (0) / LOW (1)	

Slow Control : Sel FlagTDC Ext	Slow Control : Forced_FlagTDC	Digital ASIC: FlagTDC_Int	***Flag TDC***
0	**X**	**0**	**0**
0	**X**	**1**	**1**
1	**0**	**X**	**0**
1	**1**	**X**	**1**

During conversion, Digital ASIC automatically switches FlagTDC_Int from 0 to 1 for each stored event

Table 4 – Analogue output/Converted data

5. Channel acquisition

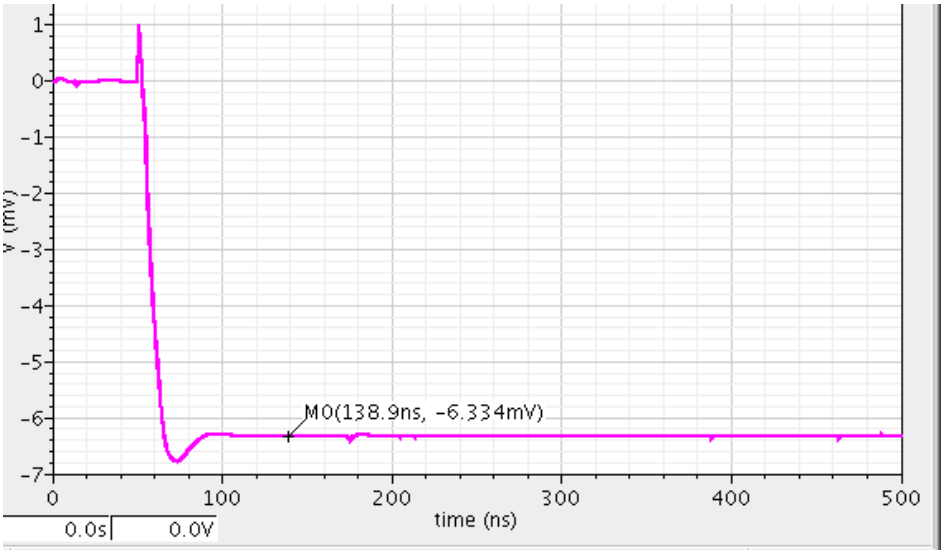
5.1. Preamplifier description

The input preamplifier is a "classical" charge preamp optimised for a 20 pF detector capacitance with a big input PMOS transistor to ensure a large g_m and a low series noise, followed by a transistor in cascode configuration.

The feedback capacitor can be varied from 400 fF up to 6 pF using the SC parameters (SC 6 to 9). The compensation capacitor can be tuned to ensure the stability using the SC parameters (SC 3, 4 and 5).

The feedback resistor of each preamp can also be set to a value bigger than 1 GΩ for leakage current of the Si diode lower than 100 pA or smaller than 60 MΩ for I leakage up to 10 nA using the SC parameter cmd_low_rf (SC 12 for ch0, SC 15 for Ch1 ..).
A bad channel can be switched off using the SC parameter dis_pa (SC 10 for Ch0, SC 13 for Ch1 …).

Most of the simulations performed were made with: C*d*=20pF, C*f*=6pF and C*comp*=6pF which is the configuration used to handle the 0.1 MIP up to 2500 MIP dynamic range.



Qinj	Out_pa
1 MIP	639.6 µV
10	6.32 mV
100	63.2 mV
200	126.4mV
500	315.9 mV
1000	631.6 mV
2000	1252 mV
2500	1465 mV

Figure 4 – PAC step response (10 MIP)

5.2. Fast channel

The fast channel is made of a high gain amplifier (G=10) followed by a variable CRRC shaper.

5.2.1. High gain amplifier

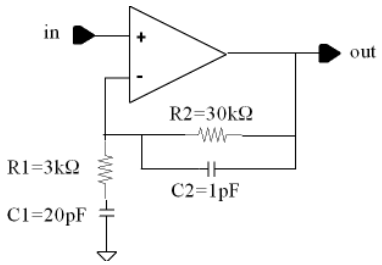


Figure 5 – Gain10 amplifier

The amplifier is a classical differential pair.

5.2.2. Fast shaper

The fast shaper that follows the high gain amplifier is a CRRC shaper the peaking time of which is tuneable between 30 ns up to 120 ns using the SC parameters (SC 207 and 208).

It is a classical design using a NPN differential pair to reduce the offset and for speed performance.

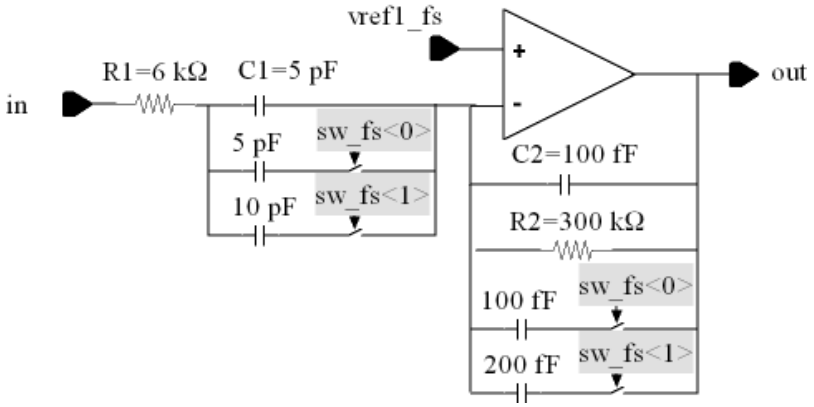


Figure 6 – Fast shaper

The response for 1 MIP at the input of the PAC (C*f*=6pF) has been simulated.

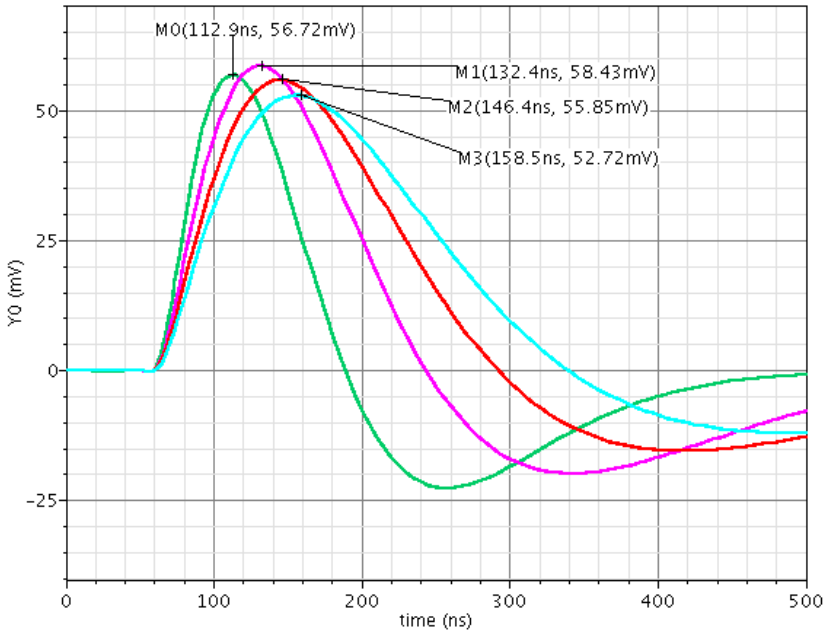


Figure 7 – 1 MIP response for various tp

	Vmax (1 MIP)	tm	Noise	S/N
6k-20p,400k-400f	51 mV	97 ns	3.2 mV	**15.9**
6k-15p,400k-300f	53.8 mV	89 ns	3.7 mV	**14.5**
6k-10p,300k-200f	57.8 mV	72 ns	4.3 mV	**13.4**
6k-5p,300k-100f	58 mV	54 ns	5 mV	**11.6**

5.2.3. Discriminator, 10-bit and 4-bit DAC

The fast shaper is followed by a low offset discriminator. The high gain of the fast channel allows to send big signals to the discriminator and thus to trigger easily on less than 0.1 MIP.

The threshold of the discriminator is set by a 10-bit DAC which is common to the 64 channels and one 4-bit DAC for each channel.

2.4mV/DAC Unit

Bb<0>, Bb<1> … Bb<9> are set using the SC parameters 575 to 585.

This 4bit-DAC allows correction for the dispersion of the 64 fast shaper pedestals. It is made of 4 switched current sources (using the SC parameters: SC 223 up to 478). The slope is 750µV/DAC unit and the maximum value is 12 mV.

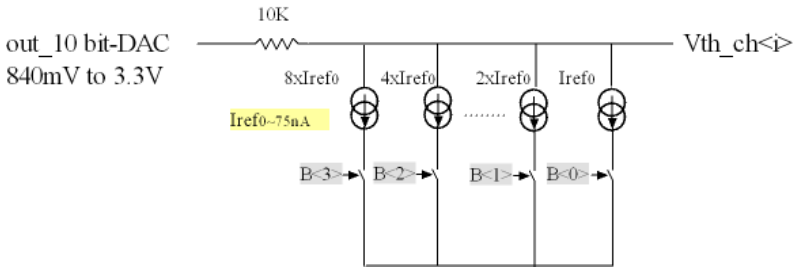


Figure 8 – 4-bit DAC per channel

5.2.4. Delay box

The discriminator is followed by an 8-bit delay cell which calibrates and delays from 100ns up to 400ns the trigger output and generates a delayed trigger used in the slow channel.

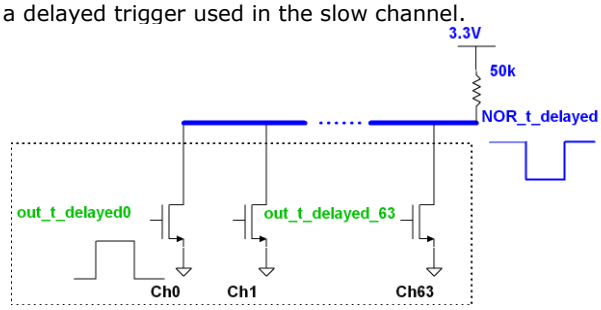


Figure 9 – outputs of the delayed triggers

The delay can be changed using the SC parameters 545 to 553. Each of the 64 delayed calibrated triggers (out_t_delayed_ch$_i$) is used to generate a "T&H" signal and also sent to an open collector transistor to generate a "NOR_t_delayed" signal used by the digital part to select the column of the SCA to be read (see 4.1.3.2 section)

	out_t_delayed
Delay<0> ON	102.4 ns
Delay<1> ON	105.5 ns
Delay<2> ON	111.6 ns
Delay<3> ON	123.3 ns
Delay<4> ON	145.7 ns
Delay<5> ON	187.7 ns
Delay<0:5> ON	261 ns
Delay<0:7> ON	419 ns

5.3. Charge and time measurements

The slow channel is made of 2 slow shapers: High gain (10) and low gain (1). Each one is followed by a 15 depth SCA for charge measurements.

5.3.1. Slow shaper

The G1 and G10 slow shapers are classical CRRC shapers. The peaking time is not variable and is equal to 180 ns.

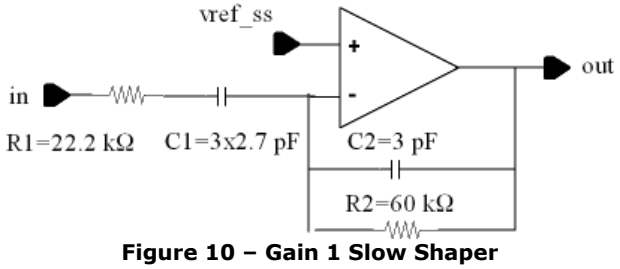


Figure 10 – Gain 1 Slow Shaper

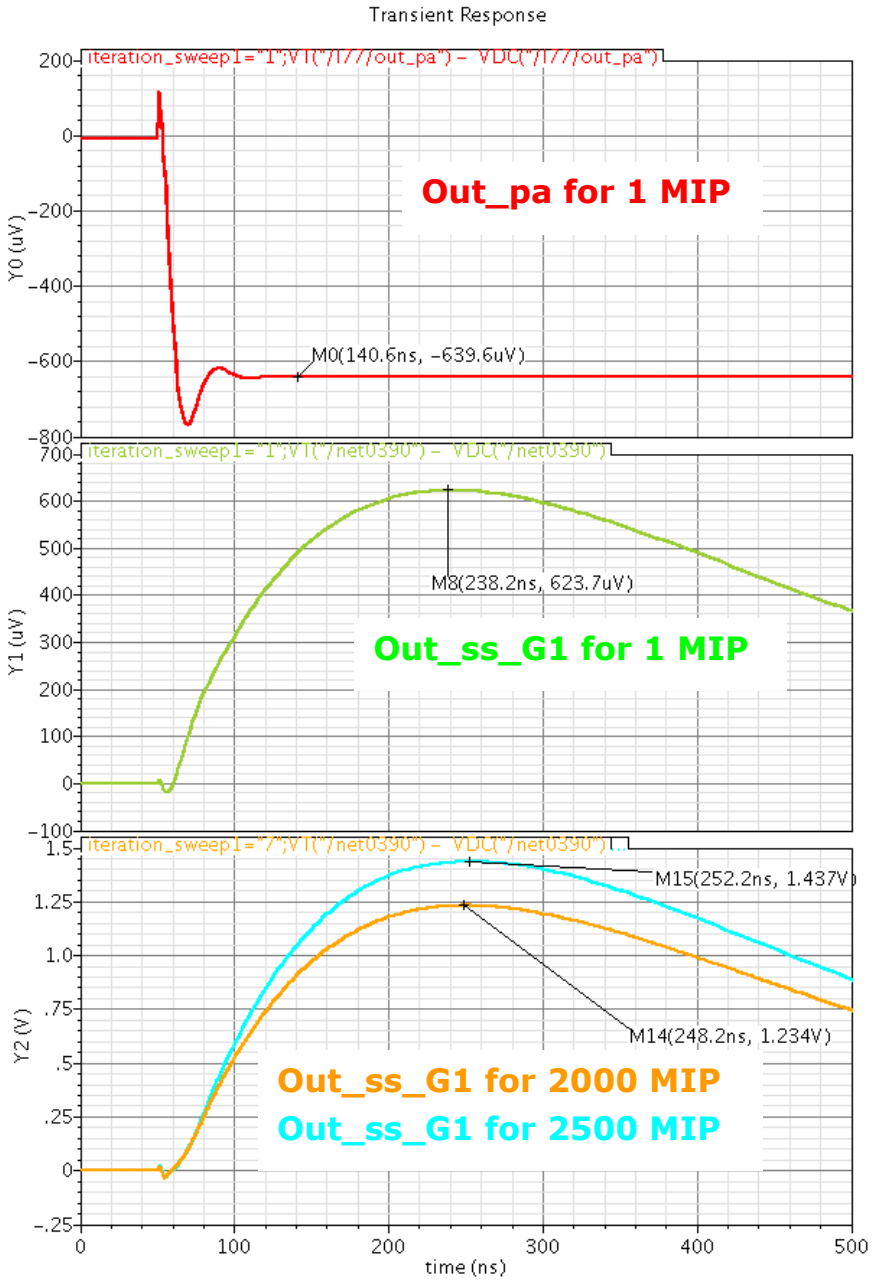


Figure 11 – Simulation of the low gain Slow Shaper for various input signals

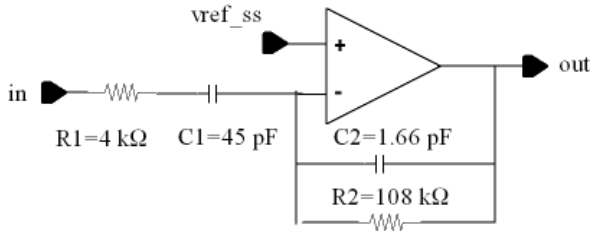


Figure 12 – Gain 10 Slow Shaper

The signal over noise ratio of the high gain shaper is 14 and is dominated by the 4kΩ resistor.

Q*inj* (MIP)	Out_pa & out_to_fs	Out_fs	Out_ss1 (G=1)	Out_ss10 (G=10)
1	635.3 µV	52.15 mV	625.1 µV	**6.11 mV**

10	6.34 mV	619 mV	6.25 mV	**61.03 mV**
100	63.34 mV	saturation	62.43 mV, tm=180ns	**609.67mV, tm=180ns**
200	126.56 mV	"	124.7 mV	**1212.9 mV**
500	315.76 mV	"	311.54 mV	**Saturation to 1.55V (+dc=1V)**
1000	630.9 mV	"	622.1 mV	"
2000	1248 mV	"	1229 mV	"
2500	**1468 mV**	**Bumps**	**1433 mV**	"

An antisaturation system has been added for the high gain shaper and has been simulated (Figure 13)

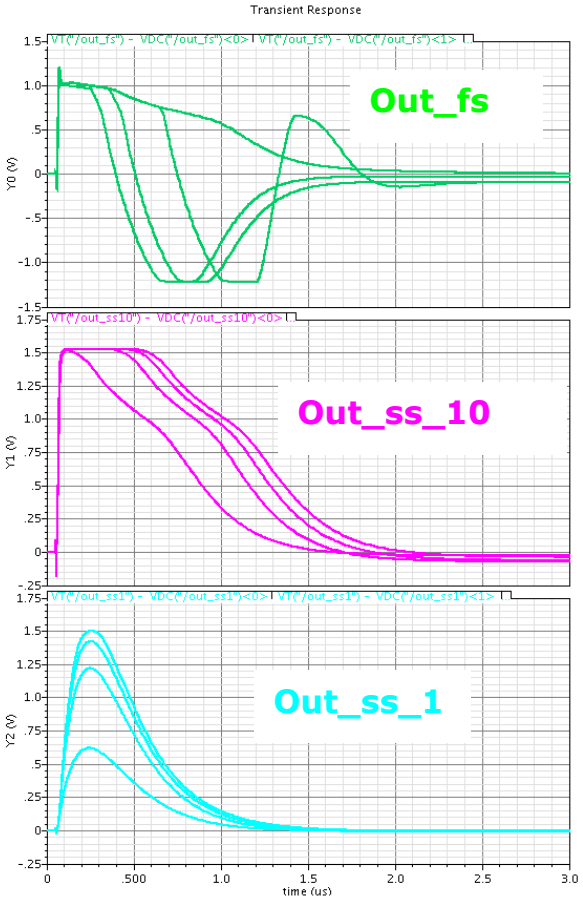


Figure 13 – 1000, 2000, 2500, 3000 MIP response

5.3.2. Time measurement

A coarse measurement is performed by a 12-bit Gray counter. The coarse time resolution is 200 ns (with a Slow Clock of 5 MHz). The time is saved in a 12-bit register as soon as there is a hit (OR64_trigger delayed).

The fine time measurement is performed by the SCA which samples the 12-bit TDC ramp which is common to all the channels.

Out_ss_1

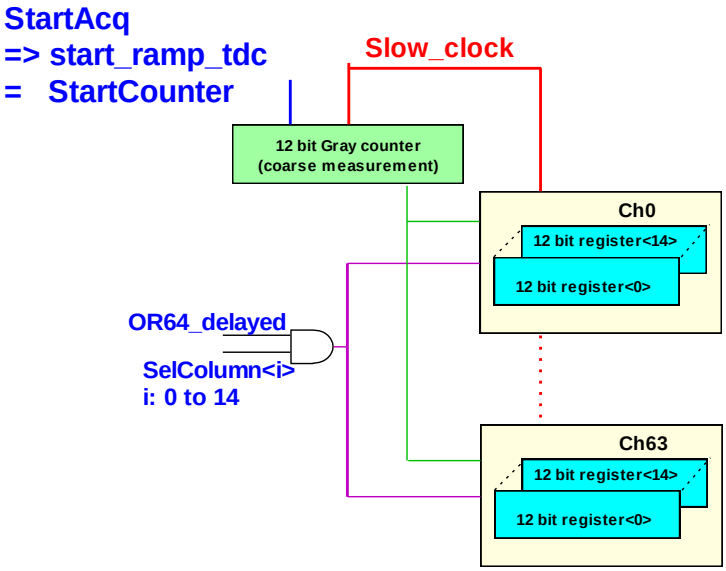


Figure 14 – Coarse measurement

5.3.3. SCA

The SCA is made of 3 Track and Hold cells, each made of 15 capacitors of 500fF, for the high and low gain charge measurement and also for the time measurement.

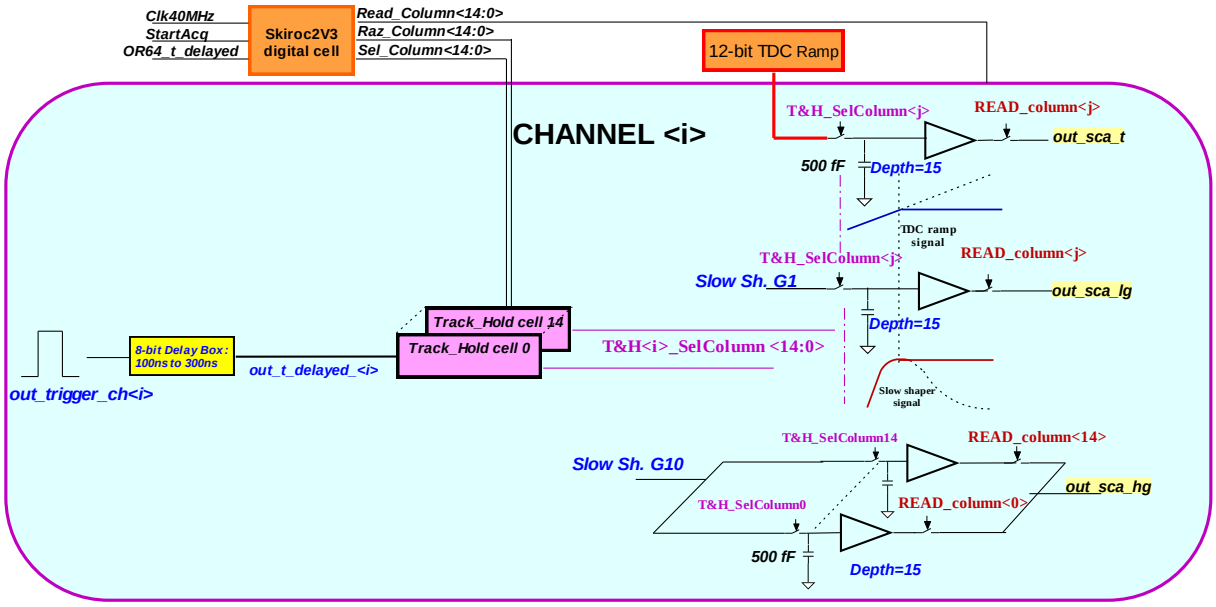


Figure 15 – SCA cell

The SCA is managed as a matrix where I is the channel number (I varies from 0 to 63) and J is the selected column to be written and read (j varies from 0 to 14).

The Track and Hold signal for each channel is generated during the acquisition phase from the delayed trigger (out_t_delayed_ch$_i$, described in section *4.1.2.4*) and the "Track and Hold" digital cell.

The selection of one of the 15 capacitors to be used for the storage is made by the "T&H_SelColumn_<14:0>" signal provided by the digital management of the overall chip (Skiroc2V3 digital cell). The selected column is the same for the 64 channels. The number of the selected column is incremented as soon as there is a trigger generated by one of the 64 fast channel that's to say as soon as a OR64_t_delayed signal has been received by the Skiroc2V3 cell.

There are 15 Track&Hold signals per channel (channel <i>: T&H<i>_SelColumn<0:14>) and the default value is "Hold". When the acquisition starts (StartAcqt="1"), the 64 T&H signals of the column0 are set to "Track".

When a trigger is generated by one of the 64 fast channels, channel<i>, the T&H<i> of the selected column j (T&H<i>_SelColumn<j>) is set to "Hold".

During the conversion phase, the capacitor to be read is selected by the Read_Column<14:0> signal generated by the digital cell Skiroc2V3 and sent to a Wilkinson ADC

6. Channel conversion

For data storage and subsequent data analysis the analog signals must be digitised. An internal Wilkinson ADC has been integrated to digitise the time and charge measurements which are stored in the SCA

An analog multiplexer selects the analog outputs to be converted depending on the "TDC_ON" signal (SC 594)

- conversion of out_sca_hg AND out_sca_lg when TDC_ON=0
- conversion of out_sca_lg or hg AND out_sca_t when TDC_ON=1

6.1. Wilkinson ADC

A 12-bit/10-bit Wilkinson ADC has been integrated as it is very suitable for multi channel application. It requires a common voltage ramp and a common counter for the 64 channels and one discriminator per channel.
The ramp and the 12/10-bit Gray counter starts as soon as a StartConv signal is sent by the DAQ (at the end of the acquisition phase).
The ADC can convert 64 charge or time values in 100µs in case of a 12-bit ADC (25µs for a 10-bit ADC). When the SCA is full, 2x15 runs are needed to convert the 2 charges or 1 charge and 1 time. The choice between a 12 or a 10-bit ADC is made using the SC parameter 593. The default value is 0 ie 12 bits.
When a conversion is over, the data are stored in a 4kbytes memory and a new conversion can start.

6.1.1. ADC ramp

The dynamic range of the ramp varies from Vref_ramp=0.9V up to 2.6V.

12 bits: Δt=102.4 µs

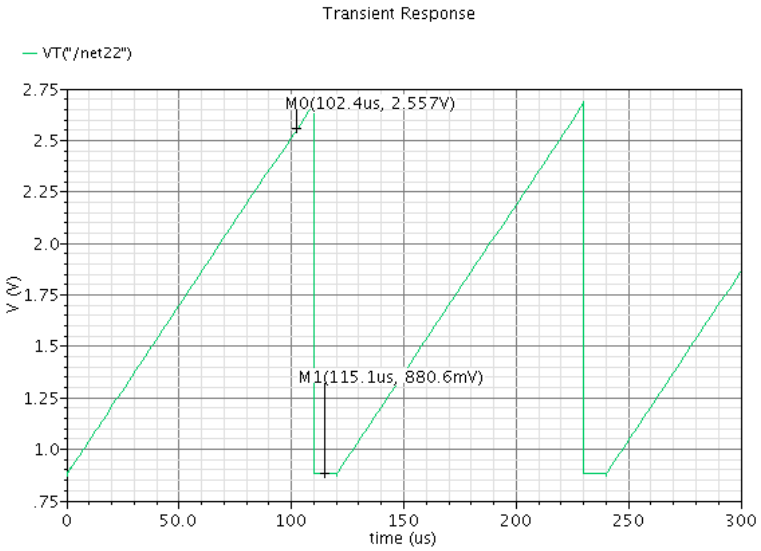


Figure 16 – 12bit ADC ramp simulation

10 bits: Δt=25.6 µs

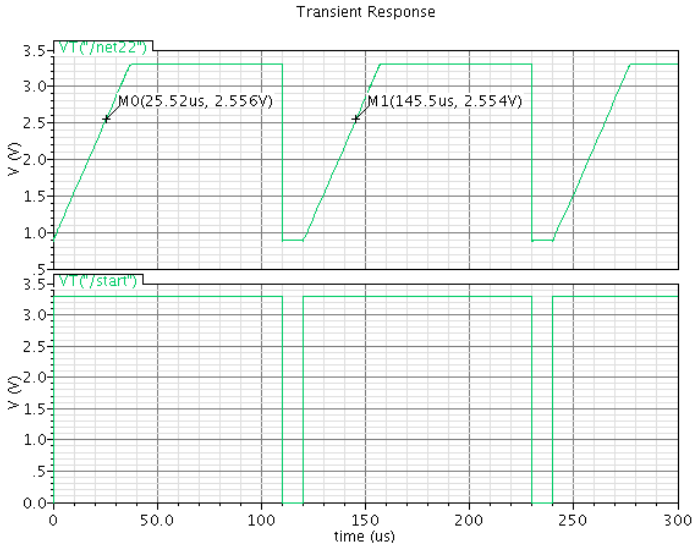


Figure 17 – 10-bit ADC ramp simulation

6.1.2. ADC discriminator

There is one discriminator per channel to compare the SCA value to the common ADC ramp.