Sk2a for CMS digital part details

1. Default value during reset state

All the inputs and outputs of the digital part are plot on the next page. The reset state is given by the signal Rstb signal @ ‘0’.

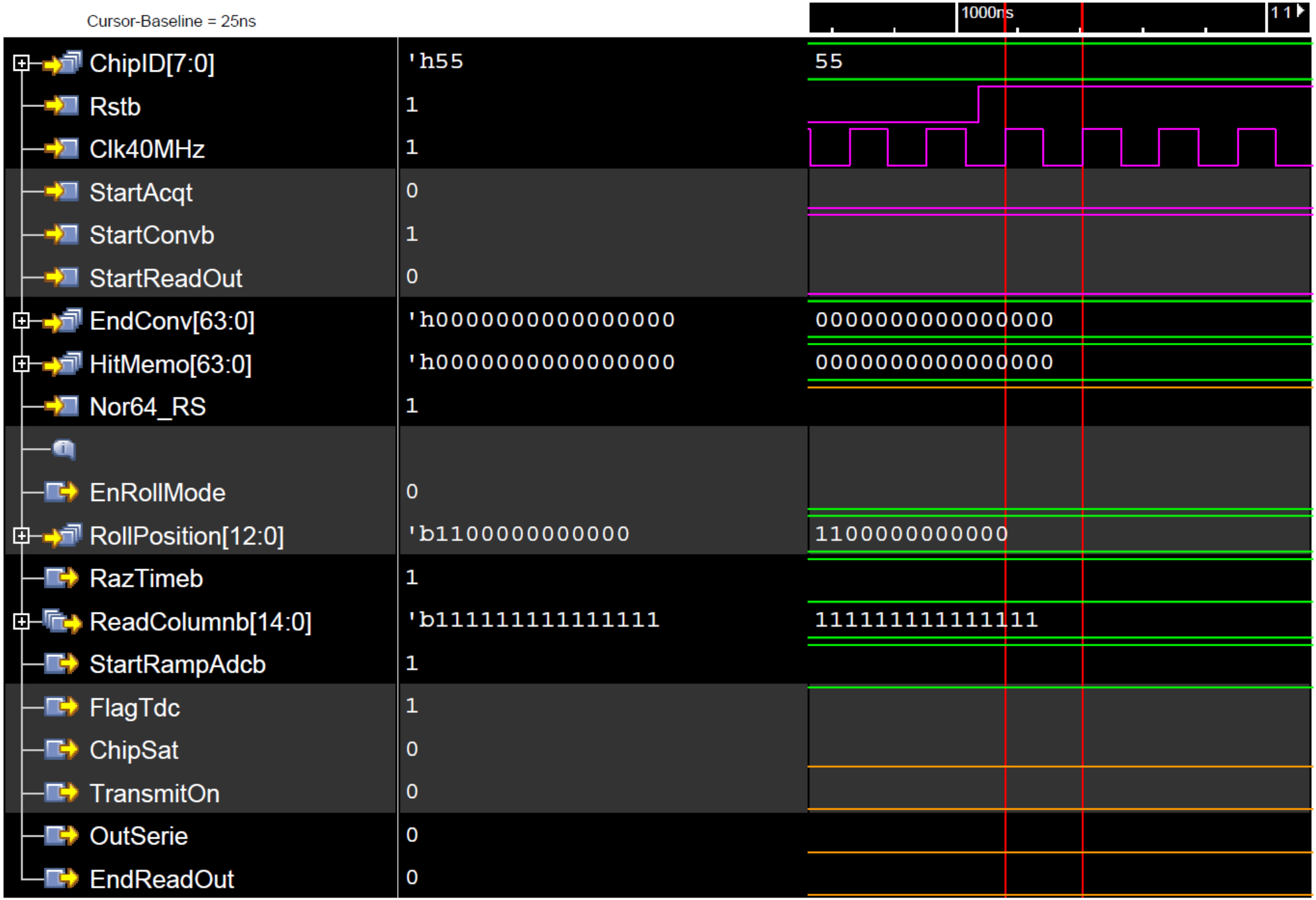
During the reset state, the outputs of the digital part are initialized (bottom part of the plot).

For example:

- OutSerie and TransmitOn signals are initialized to ‘0’
- ReadColumnb are set to ‘1’ ➔ no SCA selected for read (floating analog line to ADC discriminator)
- RazTimeb is @ ‘1’ ➔ no TOT / TOA initialization made by the digital part

The explanation of the colours are given below:

- Purple signals are provided by DAQ (Rstb, StartAcqt, StartConvb, …)
- Orange one are send to the DAQ (TransmitOn, ChipSat, …)
- Green are internal signals


Cursor-Baseline = 25ns
1000ns
ChipID[7:0]
'h55
55
Rstb
1
Clk40MHz
1
StartAcqt
0
StartConvb
1
StartReadOut
0
EndConv[63:0]
'h0000000000000000
0000000000000000
HitMemo[63:0]
'h0000000000000000
0000000000000000
Nor64_RS
1
EnRollMode
0
RollPosition[12:0]
'b1100000000000
1100000000000
RazTimeb
1
ReadColumnb[14:0]
'b111111111111111
111111111111111
StartRampAdcb
1
FlagTdc
1
ChipSat
0
TransmitOn
0
OutSerie
0
EndReadOut
0

2. Global sequence: Acquisition, Conversion and Readout

a. Acquisition and beginning of Conversion

The picture of this sequence is given below.

During the all acquisition phase, the StartAcqt signal provided by the DAQ stays to ‘1’. At the end of this phase (when the StartAcqt signal goes back to ‘0’), the ChipSat signal is set to ‘1’ to inform the DAQ that the data are ready to be converted.

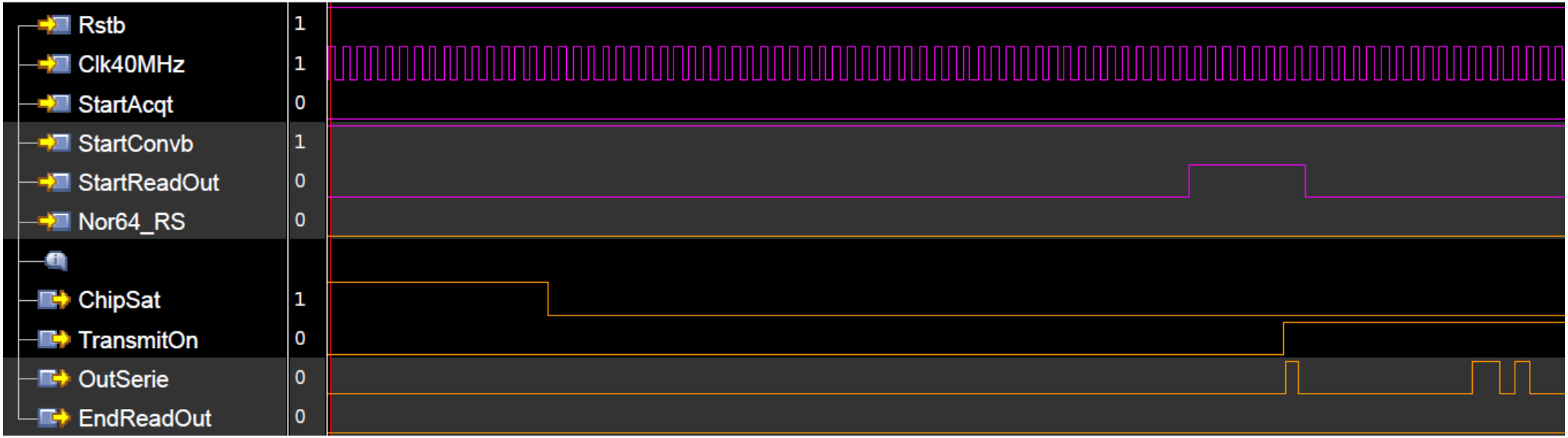
Then, the conversion is started when the digital part receives the StartConvb signal from the DAQ (negative pulse of around 250-1000 ns).

b. End of Conversion and beginning of the Readout

At the end of the conversion (total of 30 conversions), the ChipSat signal goes back to '0' to inform that the conversion process is finished.

Then, the readout is started when the digital part receives the StartReadOut signal from the DAQ (positive pulse of around 250-1000 ns).

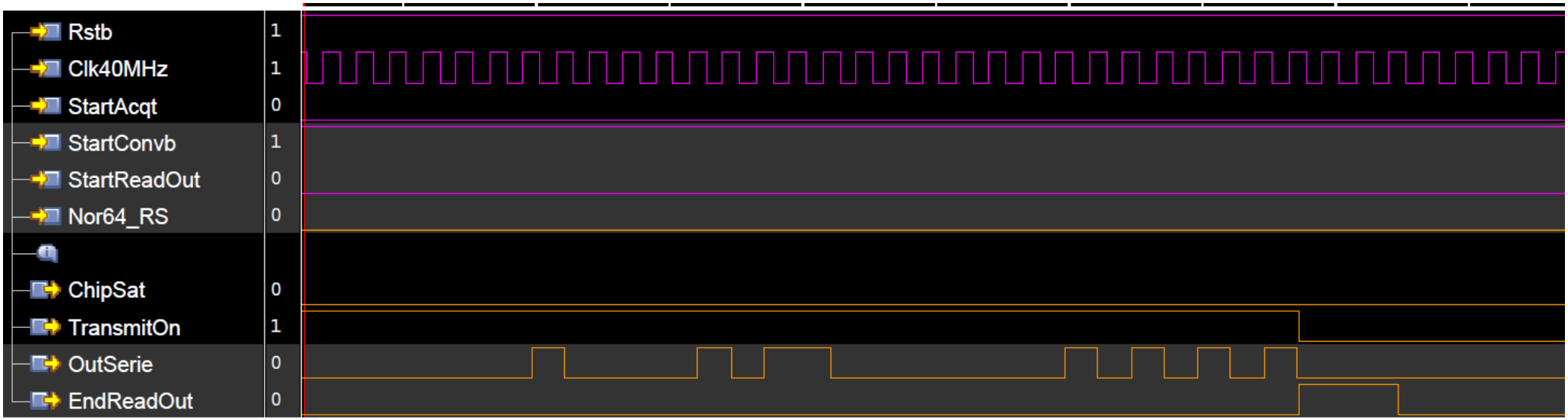
During the readout process, the TransmitOn signal is set to '1' to inform that the OutSerie line contains valid data. The TransmitOn and OutSerie signals are synchronous to the rising edge of the 40MHz clock.



c. End of the Readout

When the readout process is finished, the TransmitOn signal goes back to ‘0’. An EndReadOut pulse is also generated and outputted (75 ns pulse).

To be able to start a new acquisition, a global reset must be provided: minimum 100ns negative pulse on the Rstb signal.



3. Internal conversion process details

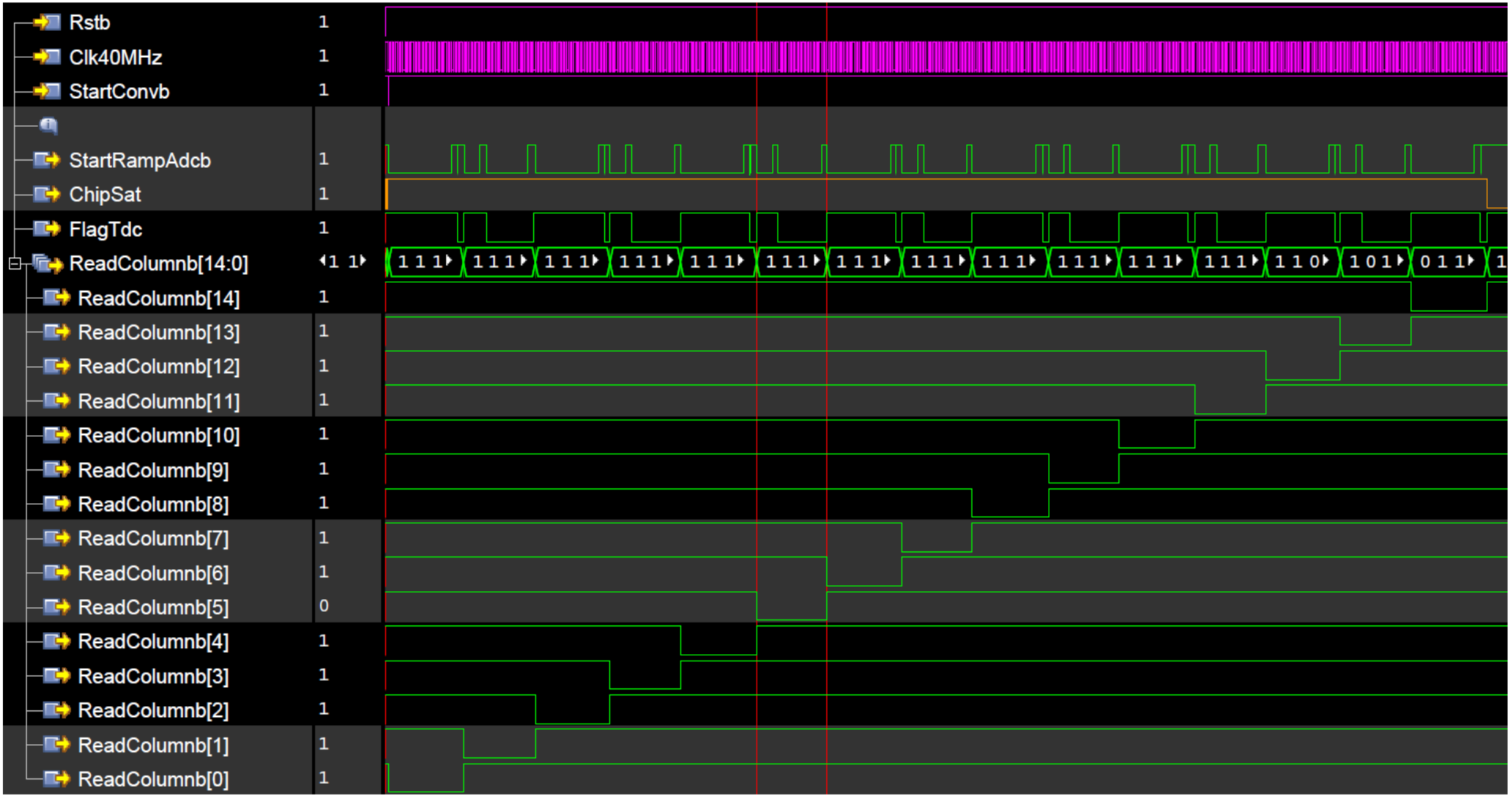
In the chip, the SCA has a depth of 15 (TOT, TOA, and 13 Q). Each depth is composed of 2 capacitors (for example HG and LG for Q).

A total of 30 conversions is needed.

An analog multiplexor 15➔1 is embedded to select the SCA depth thanks to the 15 signals ReadColumb. Another multiplexor 2➔1 is here to select the capacitor thanks to the FlagTdc signal.

The first conversion is with SCA(0) = TOT and FlagTdc @ ‘1’.

At the end of the conversion process, the ChipSat signal goes down to ‘0’.


Rstb
1
Clk40MHz
1
StartConvb
1
StartRampAdcb
1
ChipSat
1
FlagTdc
1
ReadColumnb[14:0]
1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 1
1 1 0
1 0 1
0 1 1
ReadColumnb[14]
1
ReadColumnb[13]
1
ReadColumnb[12]
1
ReadColumnb[11]
1
ReadColumnb[10]
1
ReadColumnb[9]
1
ReadColumnb[8]
1
ReadColumnb[7]
1
ReadColumnb[6]
1
ReadColumnb[5]
0
ReadColumnb[4]
1
ReadColumnb[3]
1
ReadColumnb[2]
1
ReadColumnb[1]
1
ReadColumnb[0]
1

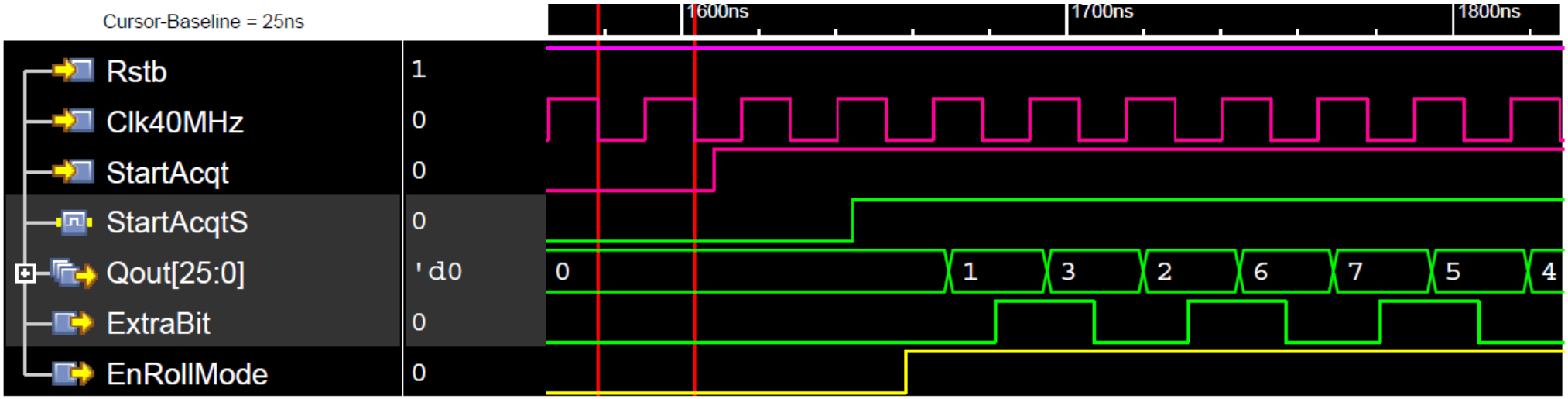
4. Beginning of Acquisition in detail

Below are the timings between the StartAcqt signal provided by the DAQ and:

- The TS counters (Qout + ExtraBit)
- EnRollMode (output)

After the StartAcqt signal, the TS counter needs 3 rising edges of 40 MHz to count.

The EnRollMode signal is synchronous with the falling edge of the 40MHz clock (the 13 SCA for Q rolls on the rising edges).



5. End of Acquisition in details

The global TS register is loaded on the falling edge of the Nor64_RS signal. The acquisition need to be stopped rapidly to prevent the digital part to erase the event.

The acquisition need to be stopped maximum 200 ns after the Nor64_RS signal goes down.