# Performing Microprocessor Programming for Microsemi ProASIC$^{PLUS}$ Devices

## Table Of Contents



## Introduction

The ProASIC$^{PLUS®}$ family of devices, Microsemi® second generation Flash field programmable gate array (FPGA), offers enhanced performance over Microsemi's ProASIC family of devices. ProASIC$^{PLUS}$ devices combine the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This combination enables engineers to create high-density systems using an existing ASIC or FPGA design flow and tools.

This application note describes the requirements to program the ProASIC$^{PLUS}$ device through a microprocessor or microcontroller using STAPL player or Microsemi's DirectC.

## Overview

User can program the FPGA using a microprocessor that is already in the system during the manufacturing process or during field upgrades. There are three main programming elements when using a microprocessor: hardware, a software program that executes the programming instructions, and programming data.

# Hardware Requirements

To facilitate programming of a ProASIC$^{PLUS}$ device, the system must have a microprocessor to process the programming algorithms, a clock source to generate TCK or RCK, memory to store the programming algorithms, programming data (Refer to Table 1 for recommended RAM size for STAPL files), and the necessary programming voltages (Refer to Table 2 on page 3 for voltage requirements). ProASIC$^{PLUS}$ devices are programmed through the JTAG port; therefore, the microprocessor must have access to the JTAG pins of the ProASIC$^{PLUS}$ device (Figure 1 on page 3).

***Table 1 •*** **Recommended RAM Size for STAPL Files**

| Device | Recommended RAM Size |
|---|---|
| APA075 | 100 kB |
| APA150 | 200 kB |
| APA300 | 250 kB |
| APA450 | 350 kB |
| APA600 | 700 kB |
| APA750 | 1 MB |
| APA1000 | 1 MB |

***Table 2 •*** **Voltage Requirements**

| Power Supply | Normal Operation | Programming Mode | Current During Programming |
|---|---|---|---|
| $V_{DD}$ | 2.5 V | 2.3 V to 2.7 V | IVDD < 20 mA at $V_{DD}$ |
| $V_{DDP}$ | 2.5 V or 3.3 V[1] | 2.3 V to 2.7 V or 3.0 V to 3.6 V | IVDDP < 20 mA at $V_{DDP}$ |
| $V_{PP}$ | 0 V to 16.5 V or floating[2] | 15.8 V to 16.5 V | IVPP < 35 mA at $V_{PP}$ |
| $V_{PN}$ | -13.8 V to 0 V or floating[3] | -13.8 V to -13.2 V | IVPN < 15 mA at $V_{PN}$ |

*Notes:*

1. *Stresses beyond the maximum voltages listed in the table may cause permanent damage to the device. Devices should not be operated outside of the Recommended Operating Conditions. Refer to the ProASICPLUS Flash Family FPGAs datasheet.*
2. *There is a nominal 40 kΩ pull-up resistor on $V_{PP}$.*
3. *There is a nominal 40 kΩ pull-down resistor on $V_{PN}$.*
4. *Absolute maximum rating on $V_{PN}$ is 0.5 V. Stresses beyond this limit may damage the device.*

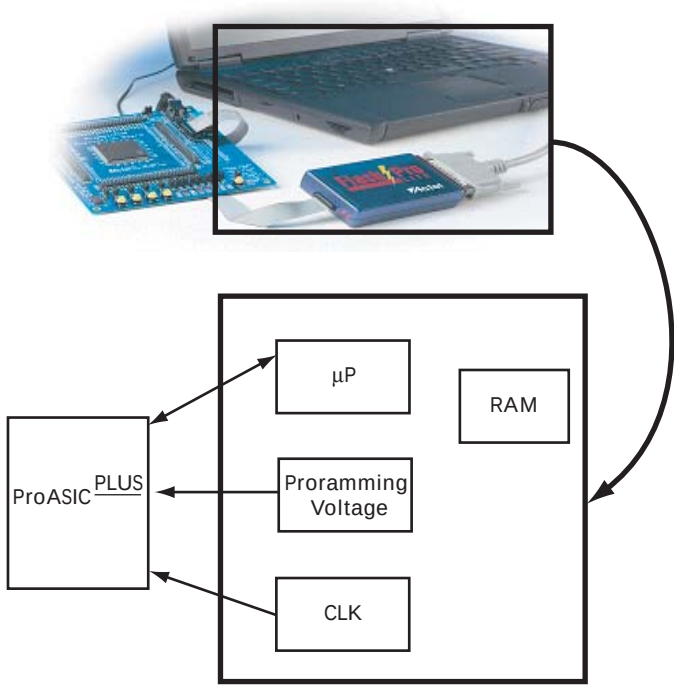


***Figure 1 •*** **Relationship Between FlashPro and an Internal System**

# DirectC vs. STAPL Software Requirements

ProASIC[PLUS] devices can be programmed using DirectC or a STAPL player. Both tools use the STAPL file as an input. DirectC is a compiled language, whereas the STAPL player is an interpreted language. Being a compiled language, DirectC is much faster to execute than the STAPL player. This speed advantage becomes more apparent when the microprocessor becomes smaller and slower.

DirectC also requires less memory than the STAPL player. However, the STAPL player does have one advantage over DirectC, the ability to upgrade. When a new programming algorithm is required, the STAPL player user only has to regenerate a STAPL file using the latest version of Designer software and download it into the system. The DirectC user must download the latest version of DirectC from Microsemi, recompile the design, and then download into the system. Refer to Figure 2 for a flow comparison of DirectC and STAPL player.

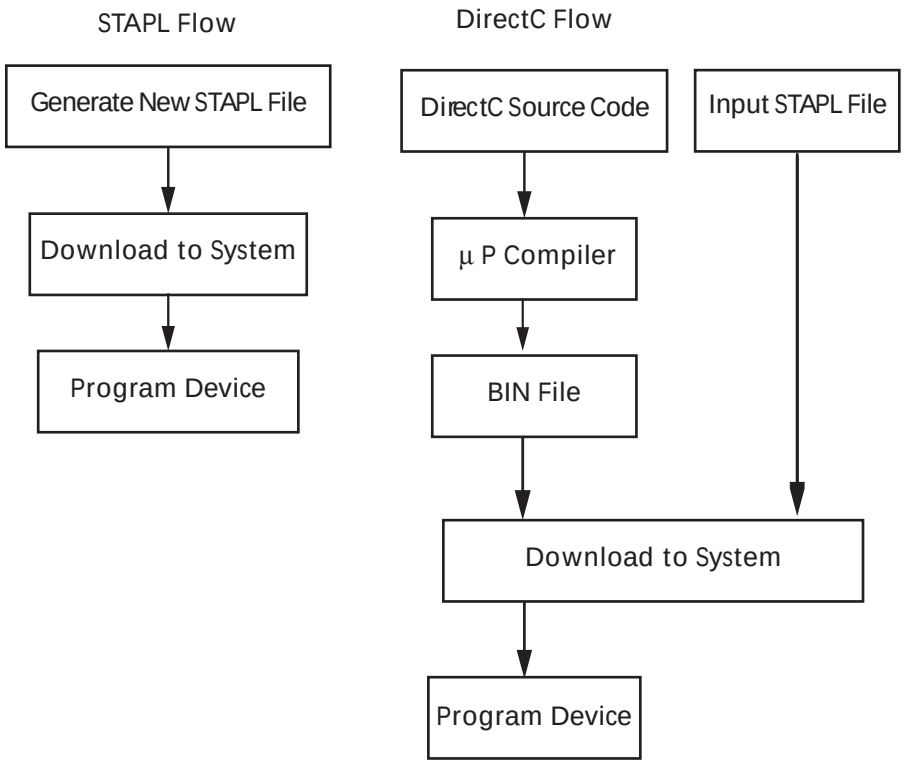


***Figure 2* • DirectC and STAPL Player Flow Comparison**

# Deployment

Both DirectC and the STAPL player can be downloaded from Microsemi's website. The DirectC and the STAPL player code from Microsemi's website are generic; they need to be modified according to the system configuration. There are two types of modifications, system-level modifications and Hardware Abstraction Layer Application Protocol Interface (HAL API) modifications.

System-level modifications are required on functions related to the system. These functions control memory allocation within the system, timing functions, clock source, and clock frequencies.

Hardware abstraction layer application protocol interface modifications are required on functions that relate to inputs/outputs. The DirectC and STAPL player code will make the JTAG level call to the HAL's API, then it is up to the HAL's API to map the JTAG calls to the low-level I/O functions.

After the necessary modifications are completed, the code will be compiled and downloaded into the system.

Refer to Figure 3 on page 5 for deployment flow.

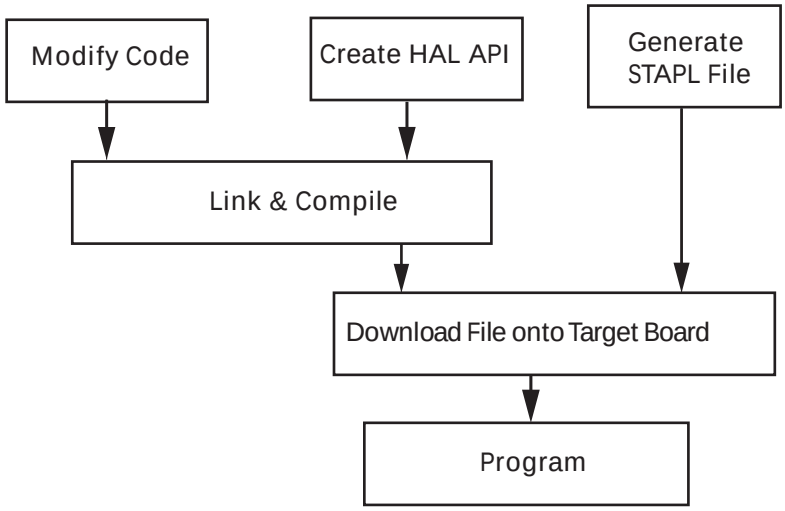


***Figure 3* • Deployment Flow**

# TCK vs. RCK

The ProASIC$^{PLUS}$ device is programmed using the JTAG port; therefore, TCK is used during normal communication between the microprocessor and the device. The Flash cells within the ProASIC$^{PLUS}$ devices require a programming pulse of a certain length. This programming pulse is self-timed by the FPGA using a continuous and non interruptible clock source. This clock can be fed into the device through TCK or RCK. If RCK is selected, the RCK clock input is only used during the programming and can be left connected during normal operations. Use RCK unless the target system can guarantee a continuous fixed frequency, TCK, which is present during waits. For most applications, RCK should be used for the programming clock to simplify the implementation of TCK.

# Conclusion

ProASIC$^{PLUS}$ devices can be programmed with a microprocessor using either DirectC or STAPL player. User can use either DirectC or a STAPL player depending on the system. If the system has a slow microprocessor and programming time, which is important to the user, then use DirectC. If programming time is not a concern for the user, then use STAPL player because it's easy to maintain.

# Related Documents

*ProASICPLUS Flash Family FPGAs datasheet*

# Appendix A: Suggested Voltage Generator Circuit

A circuit for generating the required voltages for internal ISP is shown in Figure 4 and Figure 5. Refer to Table 3 on page 7 and Table 4 on page 7 for a list of Building Materials required for building circuits. There are two Linear Tech voltage converters in the circuit. Application notes for each of them can be found at:

### *Positive Converter*

*http://www.linear.com/product/LT1930*

### *Linear Converter*

*http://www.linear.com/product/LT1931*

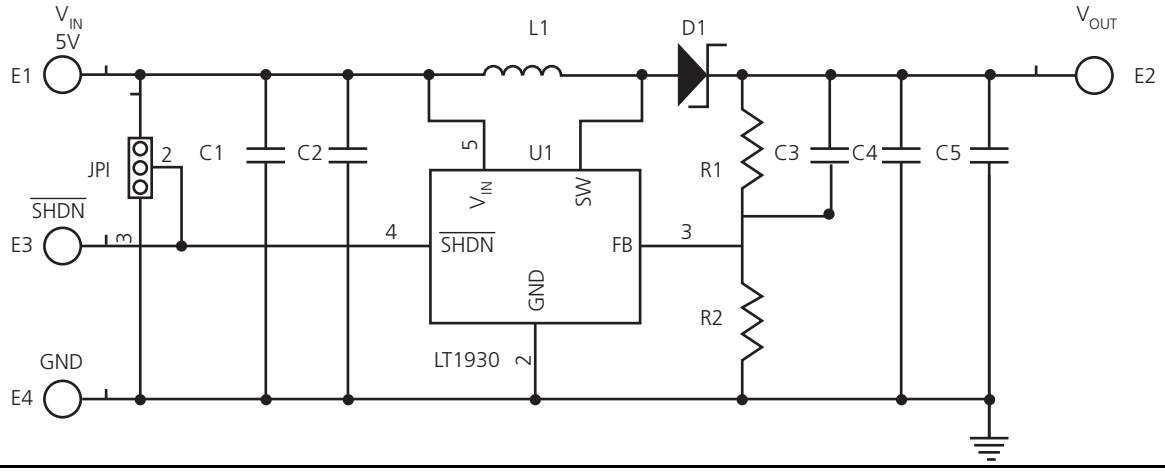


***Figure 4* • Boost Schematic**

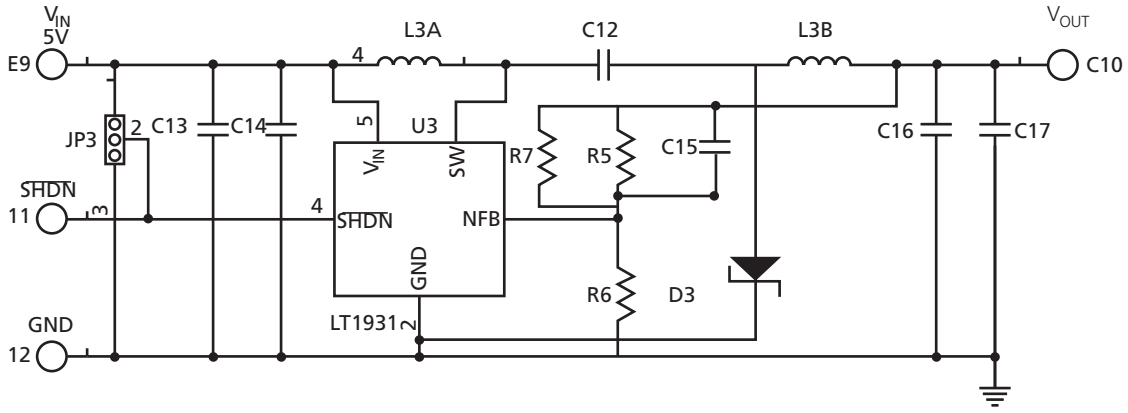


***Figure 5* • Inverter Schematic**

***Table 3 •*** **Boost Circuit**

| Item | Quality | Reference | Part Description |
|---|---|---|---|
| 1 | 2 | C1, C5 | CAP, X5R, 1 µF, 16 V, 0805 |
| 2 | 1 | C2 | CAP, X5R, 2.2 µF, 16 V, 1206 |
| 3 | 1 | C3 | CAP, NPO, 10 pF, 25 V, 10%, 0402 |
| 4 | 1 | C4 | CAP, X5R, 4.7 µF, 16 V, 1206 |
| 5 | 1 | D1 | DIO, SCHOTTKY, 30 V, 0.5 A |
| 6 | 1 | L1 | Inductor, 10 µH, 20% |
| 7 | 1 | R1 | RES, CHIP, 156 K, 1/16 W, 1%, 0402 |
| 8 | 1 | R2 | RES, CHIP, 13.3 K, 1/16 W, 1%, 0402 |
| 9 | 1 | U1 | I.C., LINEAR, LT1930ES5#25117 |

***Table 4 •*** **Inverter Circuit**

| Item | Quality | Reference | Part Description |
|---|---|---|---|
| 1 | 2 | C13, C17 | CAP, X5R, 1 µF, 16 V, 0805 |
| 2 | 2 | C14, C16 | CAP, X5R, 4.7 µF, 16 V, 1206 |
| 3 | 1 | C12 | CAP, X5R, 1 µF, 25 V, 1206 |
| 4 | 1 | D3 | DIO, SCHOTTKY, 30 V, 0.5 A |
| 5 | 2 | L3A, L3B | Inductor, 10 µH, 30% |
| 6 | 1 | R5 | RES, CHIP, 10 K, 1/16 W, 0.1%, 0402 |
| 7 | 1 | R6 | RES, CHIP, 1 K, 1/16 W, 0.1%, 0402 |
| 8 | 1 | R7 | RES, CHIP, 402 K, 1/16 W, 1%, 0402 |
| 9 | 1 | U3 | I.C., LINEAR, LT1931ES5#25118 |

# List Of Changes

The following table shows important changes made in this document for each revision.

| Revision | Changes | Pages |
|---|---|---|
| Revision 7 (October 2015) | Non-technical updates. | NA |
| | Note: Rebranded document from Actel to Microsemi therefore the history of the previous versions is not available. | |

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo,
CA 92656 USA

**Within the USA**: +1 (800) 713-4113
**Outside the USA**: +1 (949) 380-6100
**Sales**: +1 (949) 380-6136
**Fax**: +1 (949) 215-4996

**E-mail:** sales.support@microsemi.com



Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet Solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at **www.microsemi.com**.



5192691-7/10.15