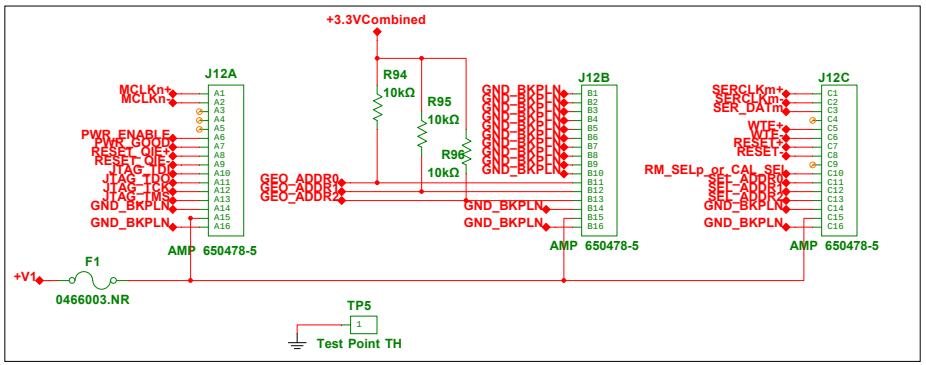
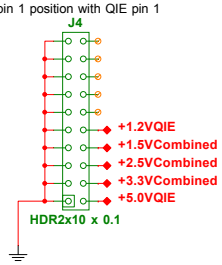
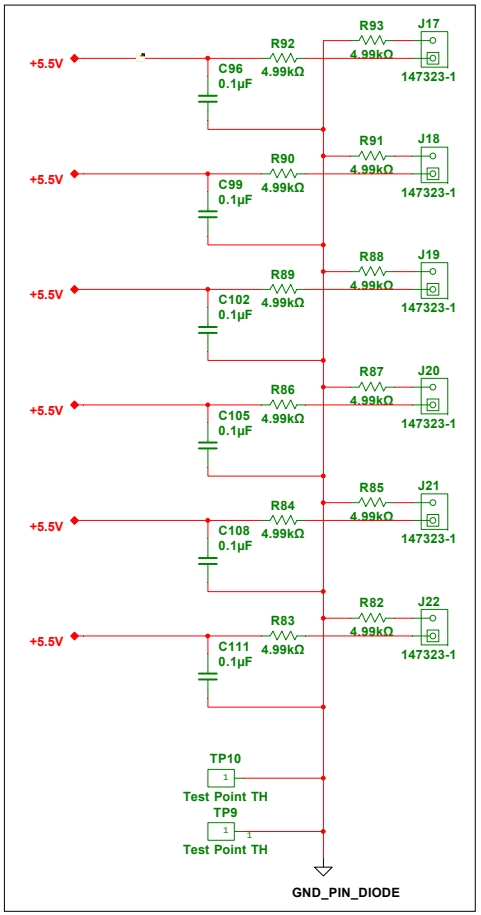
J1 BACKPLANE HEADER



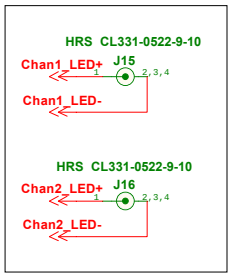
QIE board power connector
Sullins PPPC102LFBN_RC
Bottom mounted
pin 1 position with QIE pin 1



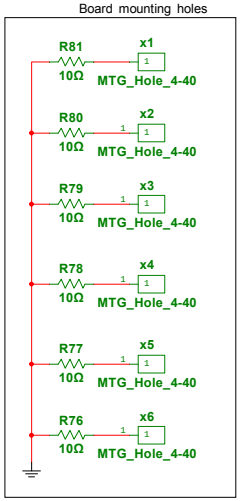
Pin Diode connections

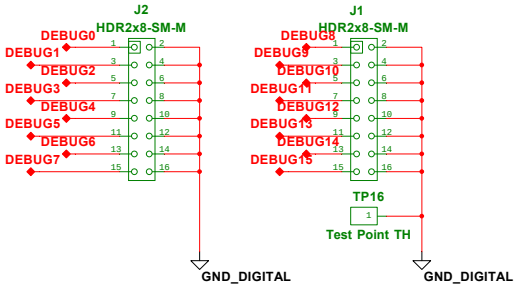


LED output connections
Coaxial cable: Hirose
H.FL-2LP(A)-111-A-(250)
245mm Minimum length
300mm closest standard length



Board mounting holes





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Project Name: HE Pulser Rev3#External connections			
Designer: © 2013, SCorkill	Page Description: HE Pulser Rev3		
Checked By:	Project Code: HEP083	Rev: 3.1	Size: C
Approved:	CAGE Code: 4B817	Date: 5/19/2016	Sheet: 1 of 13

FEASTMP_CLP modules use Samtec FTS-111-03-L-D-x
mounted to the bottom of the board with the carrier removed

R42
127k
U4
FEASTMP_CLP_5.0V
PWR_OK_QIE5.0
10µA max
DS p2-25
40µA max
PGood En
Vin Vout
PWR_ENABLE
+5.0VQIE
+V1
R54
220k
U2
FEASTMP_CLP_3.3V
PWR_OK_QIE3.3
PWR_ENABLE
+3.3VCombined
R43
82.5k
Rev3
Improved PGood signal
for all FEASTMP_CLP
and removes FPGA pullups
U3
FEASTMP_CLP_2.5V
PWR_OK_QIE2.5
PWR_ENABLE
+2.5VCombined
R52
61.9k
R53
61.9k
U5
FEASTMP_CLP_1.2V
PWR_OK_QIE1.2
PWR_ENABLE
+1.2VQIE
GND_DIGITAL

+V1
R51
10kΩ
PWR_INH_5.5
Q2
BST82215
PWR_ENABLE
GND_DIGITAL

SC2
LHC4913_Circuit
R48
18KΩ
+V1
Vin Vout
SH-CNTRL+
SH-CNTRL R2+
R45
590k
PWR_INH_5.5
OCM GND_V
INH R2-
R49
8.66kΩ
C19
10uF
+5.5V
PWR_OK_5.5
R47
249kΩ

SC1
LHC4913_Circuit
R72
18KΩ
+3.3VCombined
PWR_OK_1.5
PWR_INH
R65
560Ω
C1
10uF
C43
22.0µF
+1.5VCombined

+V1
R121
10kΩ
PWR_INH
Q1
BST82215
PWR_OK_QIE3.3
R44
4.22kΩ
Rev3
R44 no longer a board mod.
GND_DIGITAL

GROUND NET BRIDGE PLACED ON BOARD
AT BACKPLANE CONNECTOR
GND
GND_L
GND_PIN_DIODE
GND_DIGITAL
GND_BKPLN

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Project Code:	HEP083
Rev:	3.1
Size:	C
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Sheet:	2 of 13

FPGA VCC decoupling

+1.5VCombined

"Board-Level Considerations" section on page 337 of Fabric guide

C93 0.01uFFPGA
C29 0.01uFFPGA
C28 0.01uFFPGA
C26 0.01uFFPGA
C25 0.1uFFPGA
C23 0.1uFFPGA
C18 0.1uFFPGA
C74 0.01uFFPGA
C71 0.01uFFPGA
C27 0.01uFFPGA
C12 0.01uFFPGA
C24 0.1uFFPGA
C22 0.1uFFPGA
C15 0.1uFFPGA
C45 1.0µF
C46 1.0µF

U16PWR_GND

VCC F7,F8,F9,F10,G6,G11,H6,H11,J6,J11,K6,K11,L7,L8,L9,L10

QGND B3,D5,D12,N5,N12,R15

GND A1,A16,F6,F11,G7,G8,G9,G10,H7,H8,H9,H10,J7,J8,J9,J10,K7,K8,K9,K10,L6,L11,T1,T16

A3P1000L-FG256

GND_DIGITAL

LED Driver decoupling

+5.5V_L

C34 0.1µF
C35 0.1µF
C36 0.1µF
C47 0.1µF
C48 0.1µF

GND_L

Bank 0

+2.5VCombined

C117 0.1uFFPGA
C118 0.01uFFPGA
C120 0.01uFFPGA
C122 0.01uFFPGA
C124 0.01uFFPGA
C125 0.1uFFPGA

GND_DIGITAL

+5.5V

LED Driver decoupling

+5.5V_L

R17 10Ω_1206
R34 10Ω_1206
C42 0.1µF
C41 0.1µF
C40 0.1µF
C39 0.1µF
C38 0.1µF
C37 0.1µF

GND_PIN_DIODE

GND_L

Bank 1

+3.3VCombined

C123 0.1uFFPGA
C121 0.1uFFPGA
C126 0.01uFFPGA
C127 0.1uFFPGA
C128 0.01uFFPGA
C129 0.1uFFPGA

GND_DIGITAL

Bank 2

+3.3VCombined

C130 0.01uFFPGA
C131 0.1uFFPGA
C132 0.01uFFPGA
C133 0.1uFFPGA
C134 0.01uFFPGA
C135 0.1uFFPGA

GND_DIGITAL

Bank 3

+3.3VCombined

C112 0.01uFFPGA
C113 0.1uFFPGA
C114 0.01uFFPGA
C115 0.1uFFPGA
C116 0.01uFFPGA
C119 0.1uFFPGA

GND_DIGITAL

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Rev:	3.1
Size:	C
Approved:	
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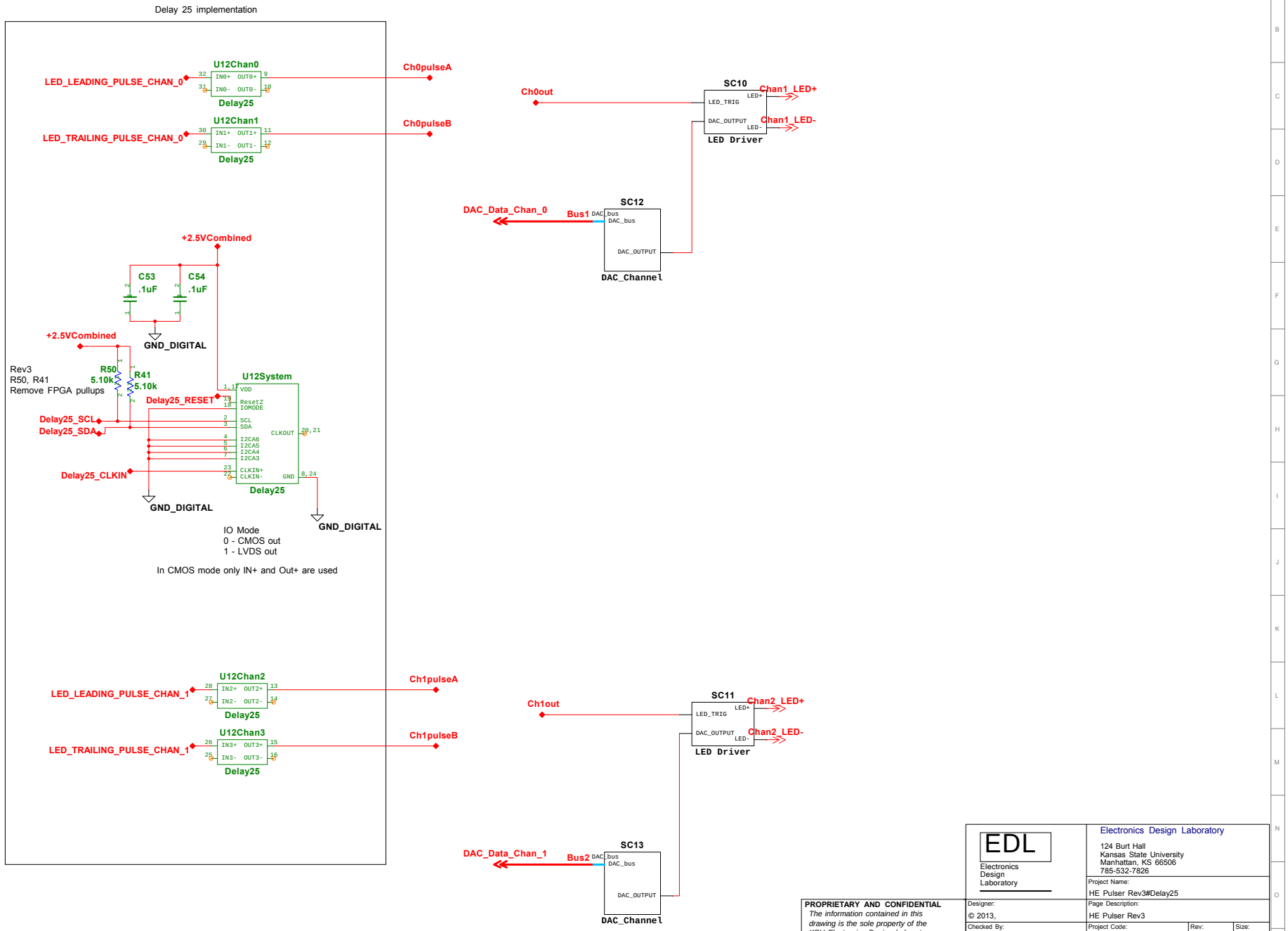
Sheet:	3 of 13



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Project Name:	HE Pulser Rev3#Delay25
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Page Description:	HE Pulser Rev3
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Project Code:	
Rev:	3.1
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CAGE Code:	4B817
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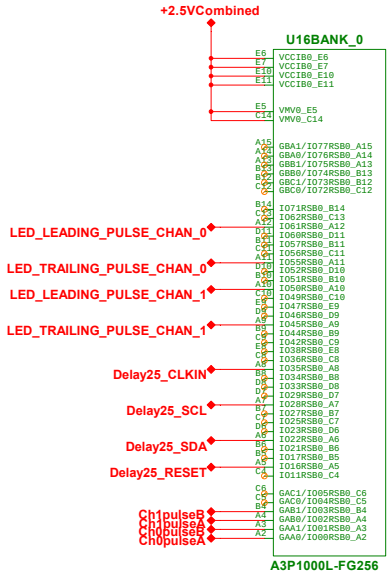
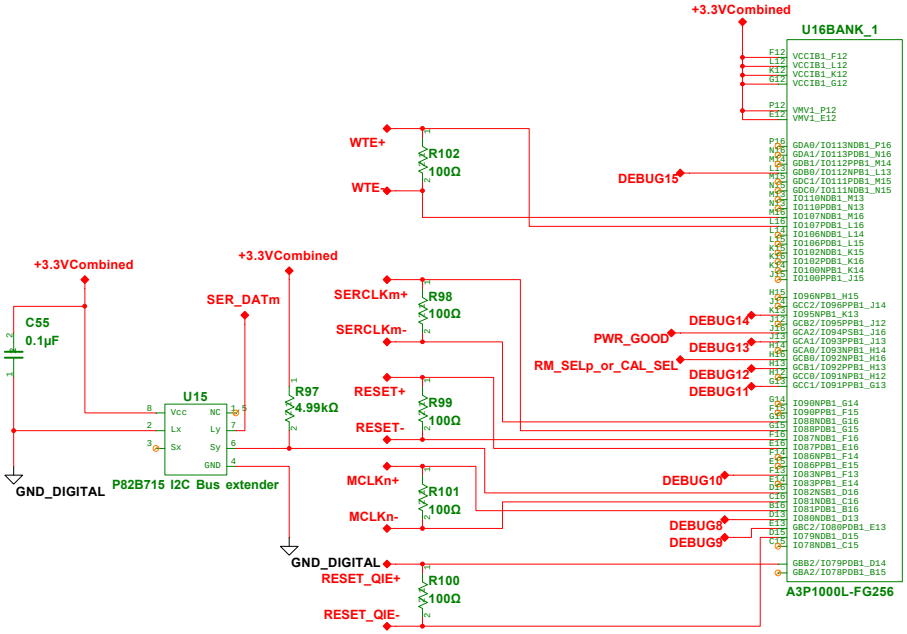
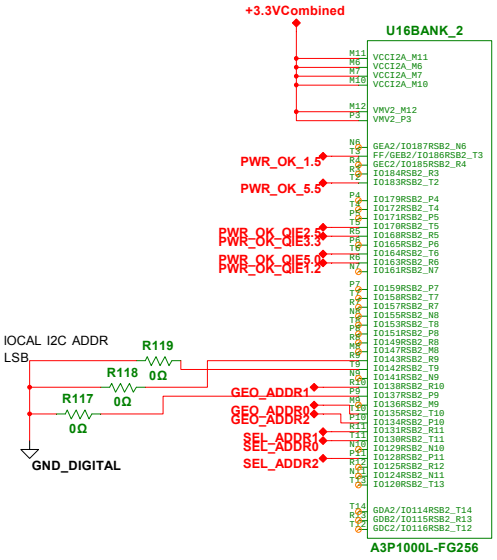
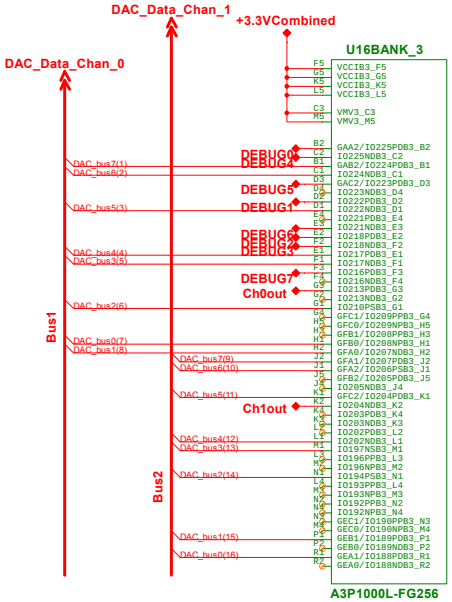
Sheet:	4 of 13

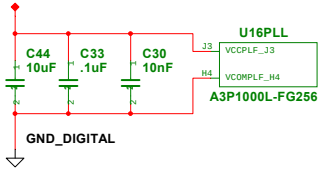
Bank 0 used for interface with the Delay25 chip which is 2.5V CMOS.
This bank's I/O Standard is LVCMOS 2.5/5.0 V. This standard is similar to LVCMOS 2.5 V,
with the exception that it can support up to 3.3 V on the input side (2.5 V output drive).











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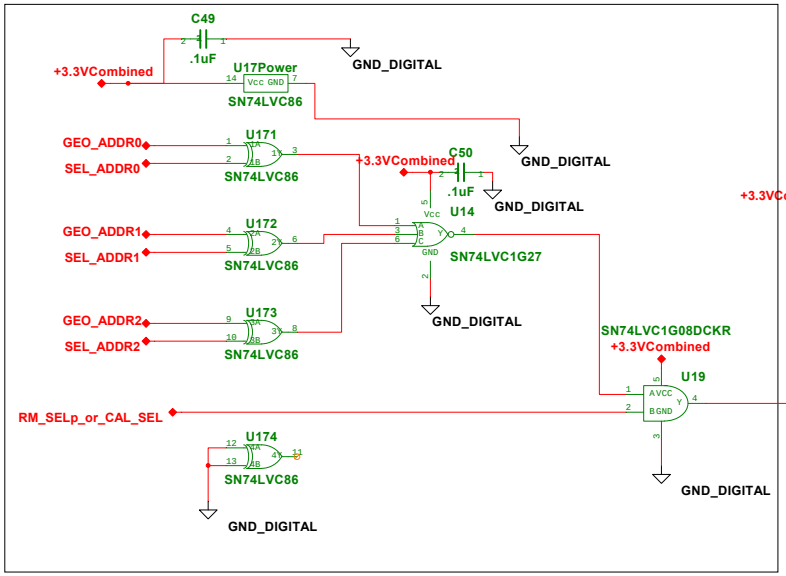
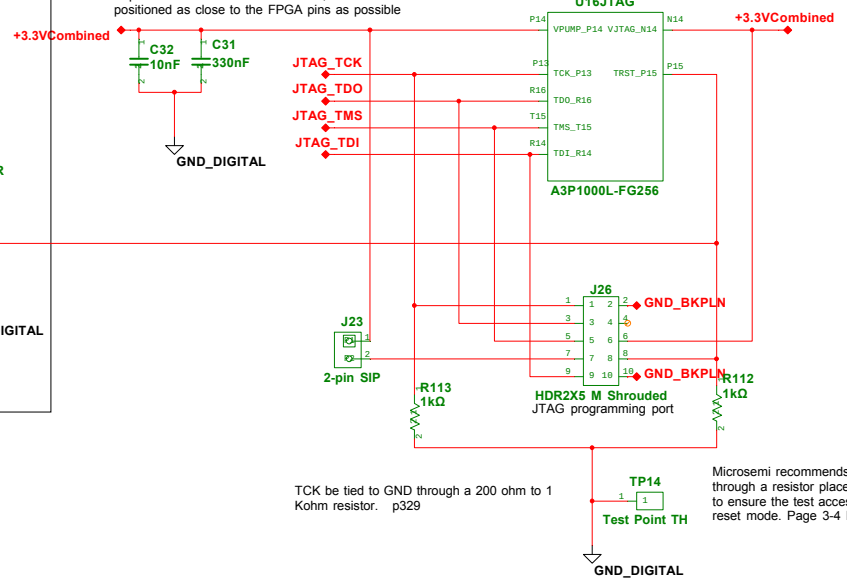
Backplane JTAG address decoding



ProASIC3L Fabric Guide Page 337
For proper programming, 0.01 µF and 0.33µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible

JTAG header information
Page 335 ProASIC3L
Fabric user guide



TCK be tied to GND through a 200 ohm to 1 Kohm resistor. p329

Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin to ensure the test access port (TAP) is held in reset mode. Page 3-4 PA3L_DS.pdf

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Revision 1

Sergey V Los version

Revision 2.0 July 2015

EDL prototype released July 2 2015

Revision 2.1

Added 0154005.DR Fuse inbetween V1 and the backplane connector J12.
Removed ferrite beads from Pin Diode connections.
Replaced Power Enable logic gates with Rad-Hard MOSFET BST82215.
Removed the logic gate for Igloo-enable.
Removed ferrite beads from Pulser Power Regulator outputs.
Connected vsense (pin 14 documented as NC) to Vout (pins 15, 16) on regulator circuits.
Changed Bank_0 to +2.5v.
Changed Bank_2 to +3.3v.
Replaced 3-input AND on GEO/SEL_ADDRESS's decoding to SN74LVC1G27 3-input NOR.
Made extra page for documenting changes. (This page)
Replaced SN74LVC1G08DCKR 2-input AND gates with on-chip logic on FPGA.
Changed the pin for Debug1-4, and for the two AND gates.
Changed R97 on I2C buffer from 100k to 5k
Corrected Symbol pin error on FPGA where Bank2 contained D14 and B15 from Bank1

Revision 2.2 DC-DC converters. October 2015

Combined power supplies from 9 LHC4913s to
    2 LHC4913 and
    4 FEASTMP_CLP DC-DC converters
Added EDL label
Added to project Daughter board LMZ31704 DC-DC converter to standin for the
    FEASTMP_CLP until it becomes available in December
Removed connections to QIE V1 on connector J4

On board modifications to Revision 2.2 (Rev2.3)

November 2015:
Add voltage divider resister R44 (0602 4.22kohm placed accross U6 Pin 11 and 12)
    LHC4913 (U6) V1 source is is now 3.3VCombined. 3.3V+0.5V Max input for PWR_INH
Remove R50
Replace R41 with zero ohm.
        With V1 now 3.3VCombined OCM no longer needs the
        R50 and R41voltage divider to reduce 11V to 3.3V

March 2016:
FEASTMP_CLP PowerGood sink current <50µA. For FPGA LVTTL 3.3V,
the pull-up resistor is ~45 kΩ (p191 ProASIC3L Fabric User Guide).
VIH = 2Vmin VIL = 0.8max (p2-22PA3L_DS)
Using FPGA pullup = (3.3-0.8)/45kΩ=55.5µA. exceeds max sink
Using 2.5V supply for pullup (2.5-0.75)/45µA = 39kΩ.
        Add R53 39kΩ from 2.5V to U5 (1.2V) pin1 (PWR_OK_QIE1.2)
        Add R53 39kΩ from 2.5V to U3 (2.5V) pin1 (PWR_OK_QIE2.5)
        Add R53 39kΩ from 2.5V to U2 (3.3V) pin1 (PWR_OK_QIE3.3)
        Add R53 39kΩ from 2.5V to U4 (5.0V) pin 1 (PWR_OK_QIE5.0)
        FPGA frimware - Remove 3.3V pullup on (in above order) R6, T5, R5, T6

Revision 3 March 2016

Include all Rev2.2 On Board modifications
Add 5kohm pullups on Delay25 I2C clock and data
Remove FPGA weak pullups for I2C clock and data
        signal is ok but will be sharper with stronger external pullups.
FEASTMP_CLP PGood signal should source <50µA from its Vout
        Remove FPGA pullups from FEASTMP_CLP PGood signals. Use with HE Pulser Firmware Rev3.
        Add R53 56.2kΩ from +2.5VCombined to U5 (1.2V) pin1 (PWR_OK_QIE1.2).
                HCAL Phase1 Upgrade meeting 31 March 2016 determined ok to allow 1.2V PGood sig
                (PWR_OK_QIE1.2) to be incorrect if 1.2V FEASTMP_CLP is completely dead i.e. derive pullup
                from +2.5VCombined rather than its +1.2VQIE. Note 1.2V cannot be used because FPGA
                needs >2V for logic high and no rad-hard level shifter is available.
        Add R52 56.2kΩ from +2.5VCombined output to U3 (2.5V) pin1 (PWR_OK_QIE2.5)
        Add R43 75kΩ from +3.3VCombined output to U2 (3.3V) pin1 (PWR_OK_QIE3.3)
        Add R42 100kΩ from +5.0VQIE output to U4 (5.0V) pin 1 (PWR_OK_QIE5.0)
        Add R54 165kΩ from U4 (5.0V) pin 1 (PWR_OK_QIE5.0) to GND.
Grounding scheme updated. Since Rev2.2 3.3V and 2.5V are combined voltages for HE Pulser and QIE11.
        However, the ground connections still indicated this separation. This revision removes QIE11 and
        Digital_GND and places these on backplane GND (net 0).
Updated Silkscreen notes to include "Rev3" and
        "Fabricated by TIFR, Mumbai, India" (per email Kajari Mazumdar 28 March 2016)

Revision 3.1 April 2016

Updated FEASTMP_CLP pullup values:
        R53 changed to 61.9kΩ
        R52 changed to 61.9kΩ
        R43 changed to 82.5kΩ
        R42 changed to 127kΩ
        R54 changed to 220kΩ
Updated silk screen to Rev 3.1

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Designer:	Project Name: HE Pulser Rev3#Changes		
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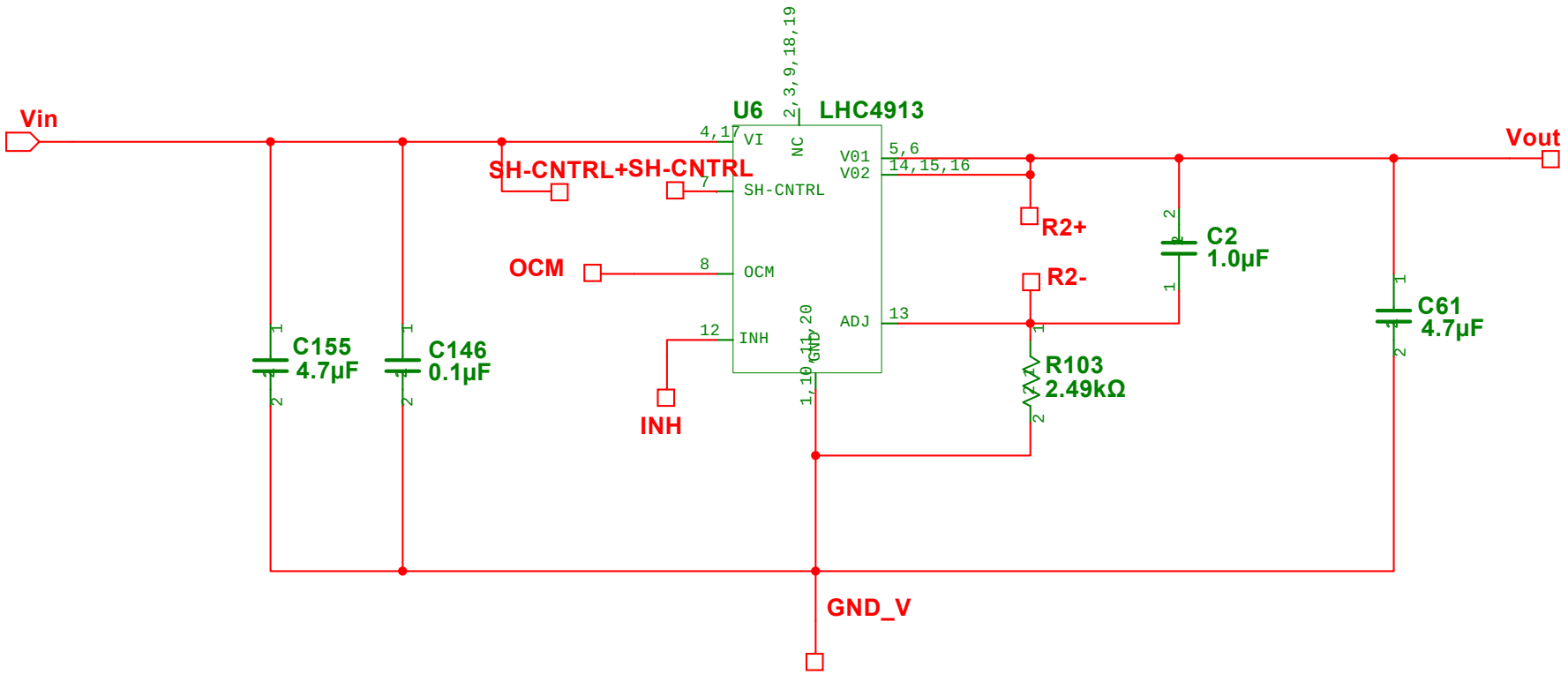

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Project Name: LHC4913_Circuit(SC1)				
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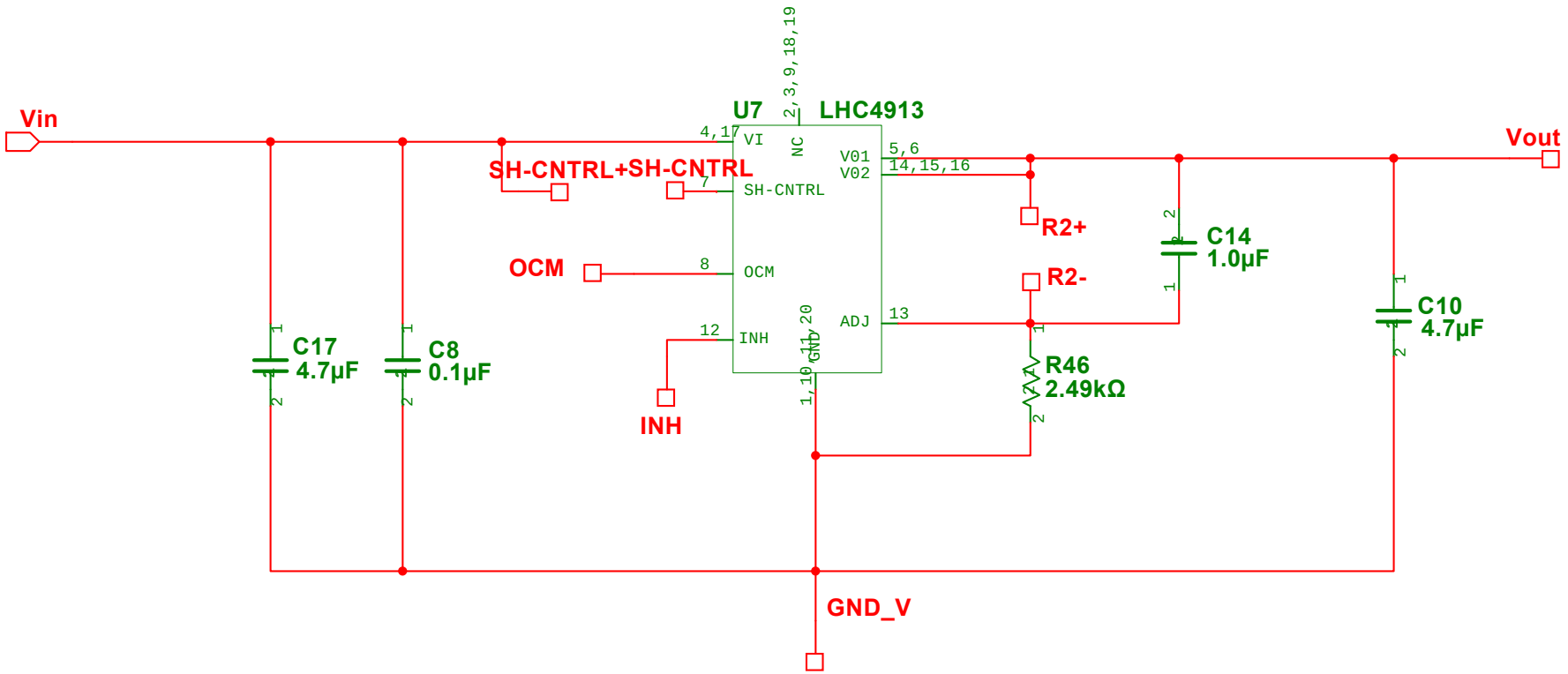
Approved:	CAGE Code: 4B817	Date: 5/19/2016	Sheet: 8 of 13	



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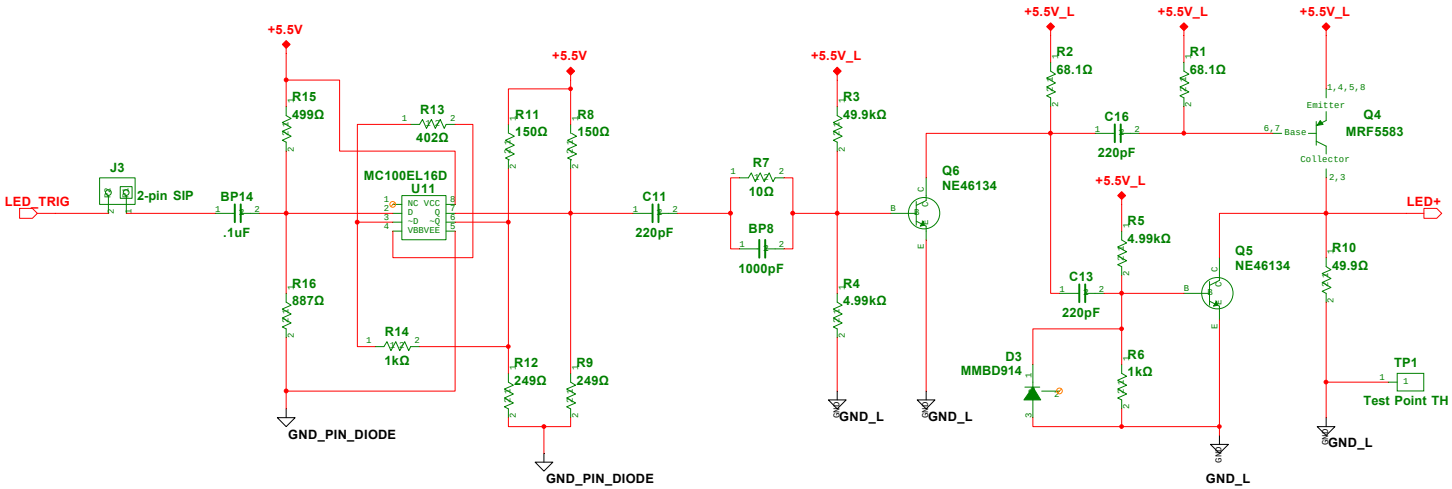

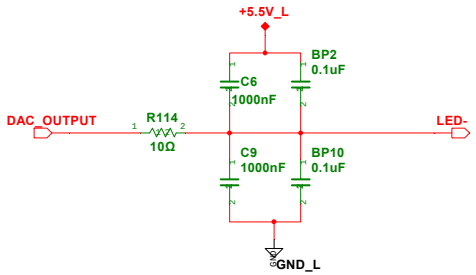

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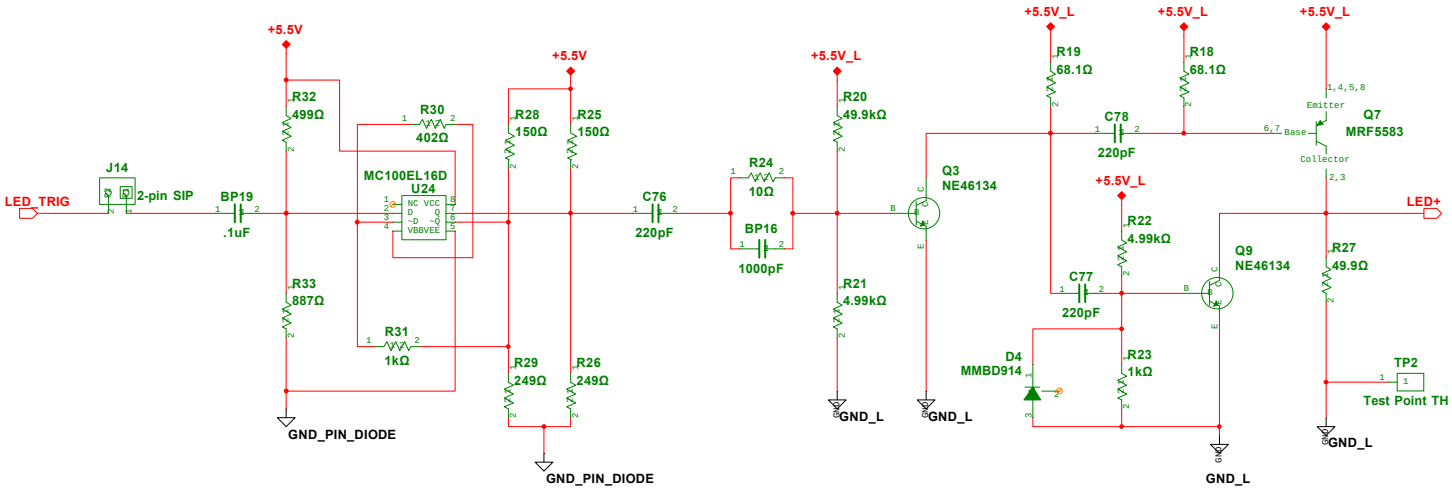

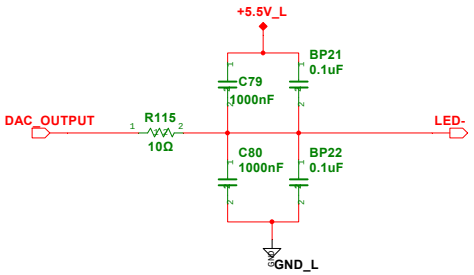

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	Project Name: LED Driver(SC11)		
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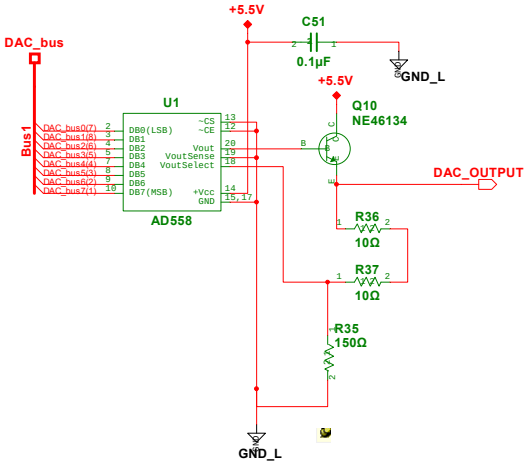

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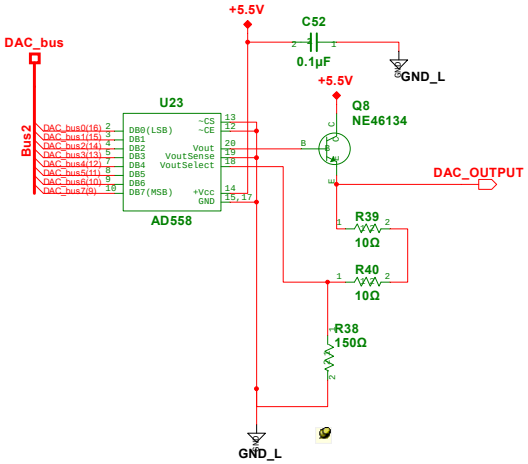

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