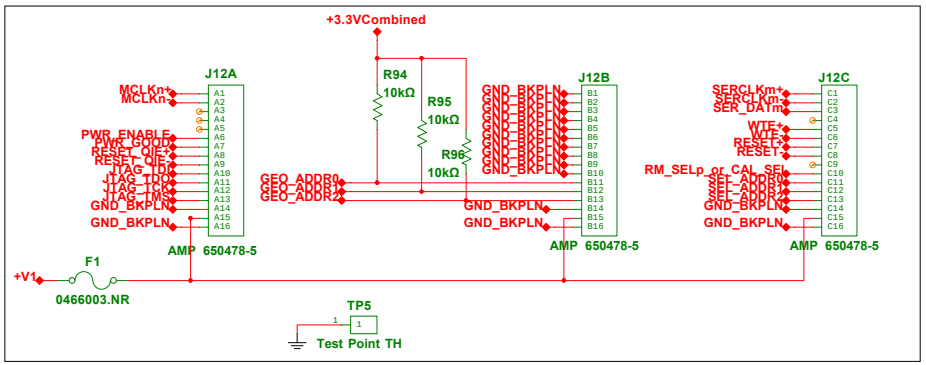
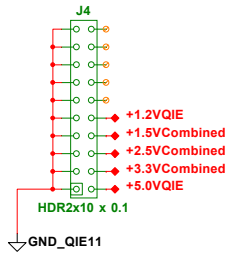
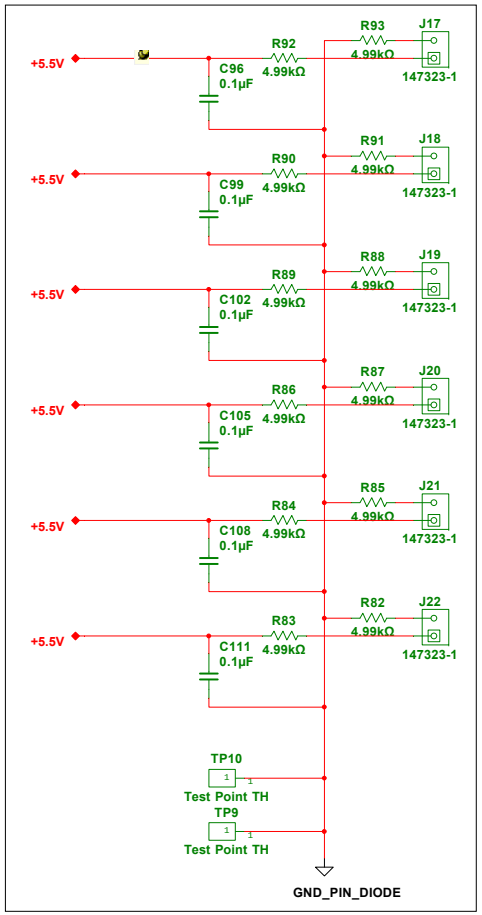
J1 BACKPLANE HEADER



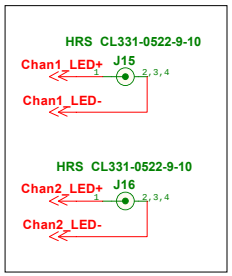
QIE board power connector
Do not populate
pin 1 position with QIE pin 1



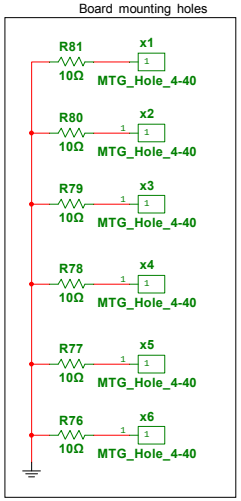
Pin Diode connections

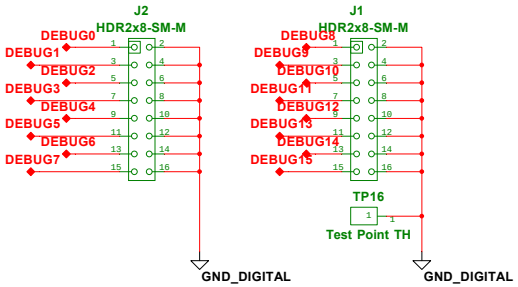


LED output connections



Board mounting holes





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Project Name:	HE Pulser Rev2_2#External connections
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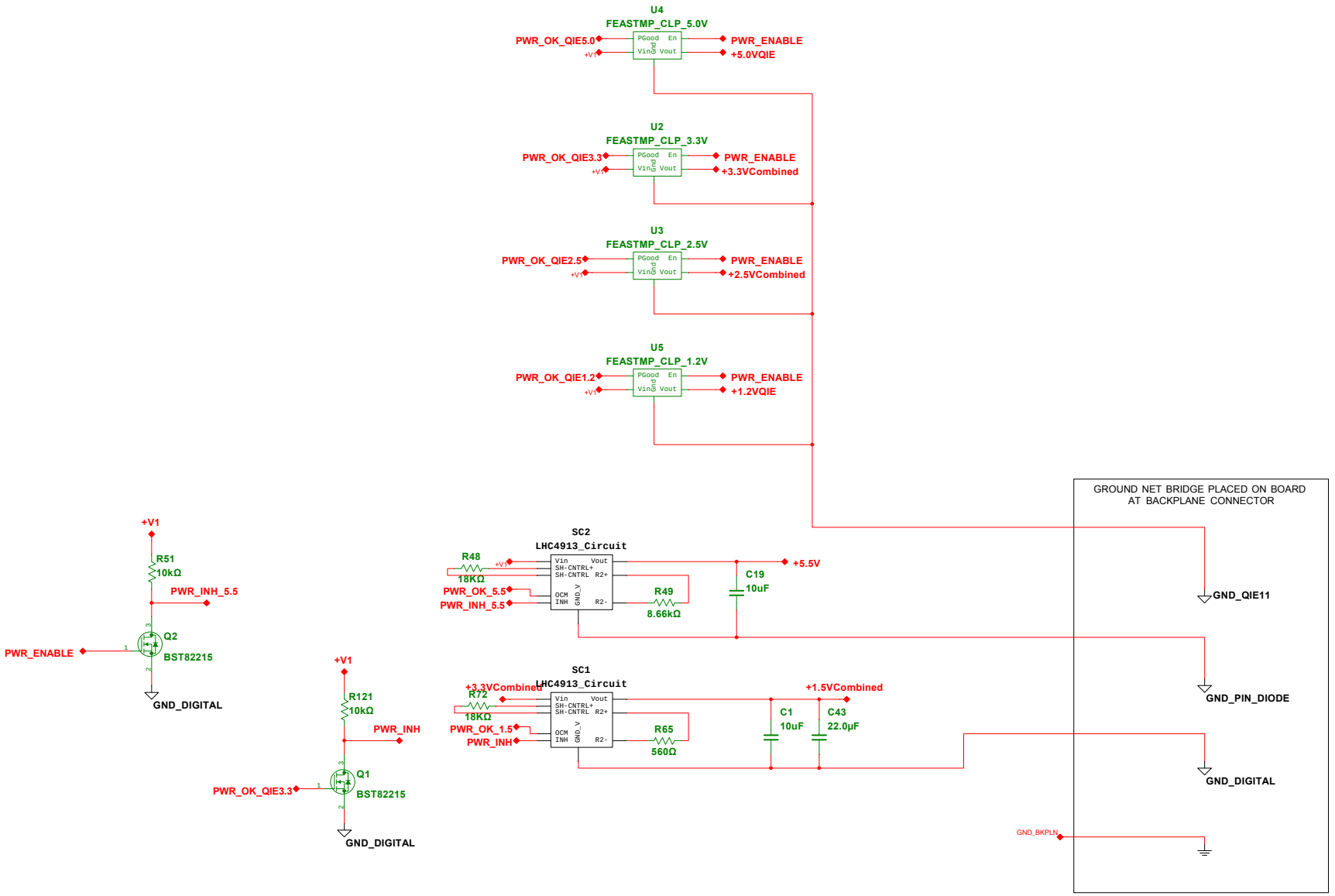
Page Description:	HE Pulser Rev2_2
Checked By:	
Project Code:	HEP083
Rev:	2.2
Size:	C
Approved:	
CAGE Code:	4B817
Date:	10/28/2015
Sheet:	1 of 13



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Project Name: HE Pulser Rev2_2#Power systems
Page Description: HE Pulser Rev2_2
Designer: © 2013, SCorkill
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Approved:
Project Code: HEP083
Rev: 2.2
Size: C
CAGE Code: 4B817
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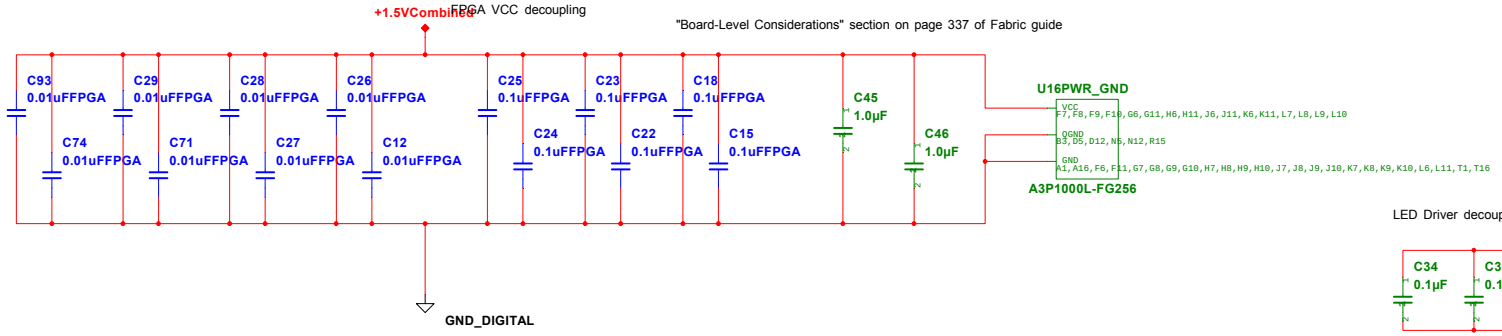
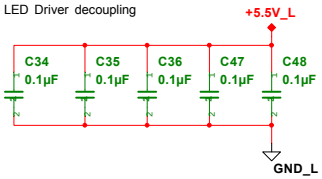
FPGA VCC decoupling

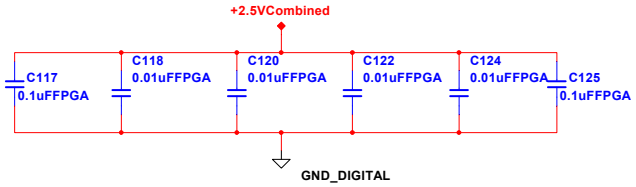
"Board-Level Considerations" section on page 337 of Fabric guide



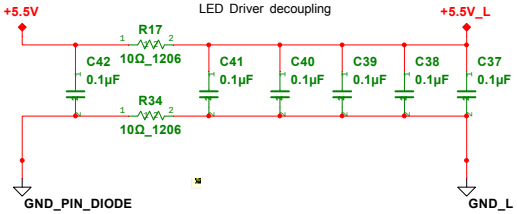
LED Driver decoupling



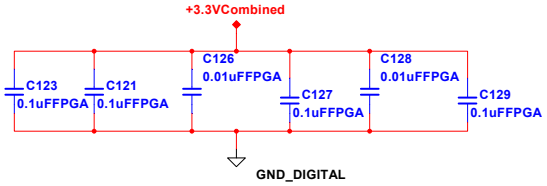
Bank 0



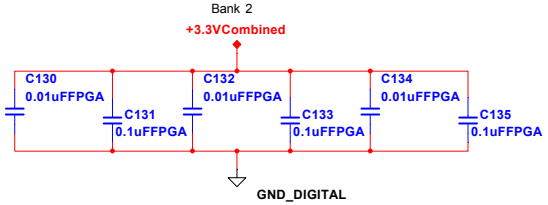
LED Driver decoupling



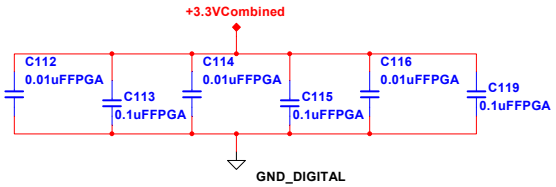
Bank 1



Bank 2



Bank 3



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Checked By:	Project Code:	Rev: 2.2	Size: C
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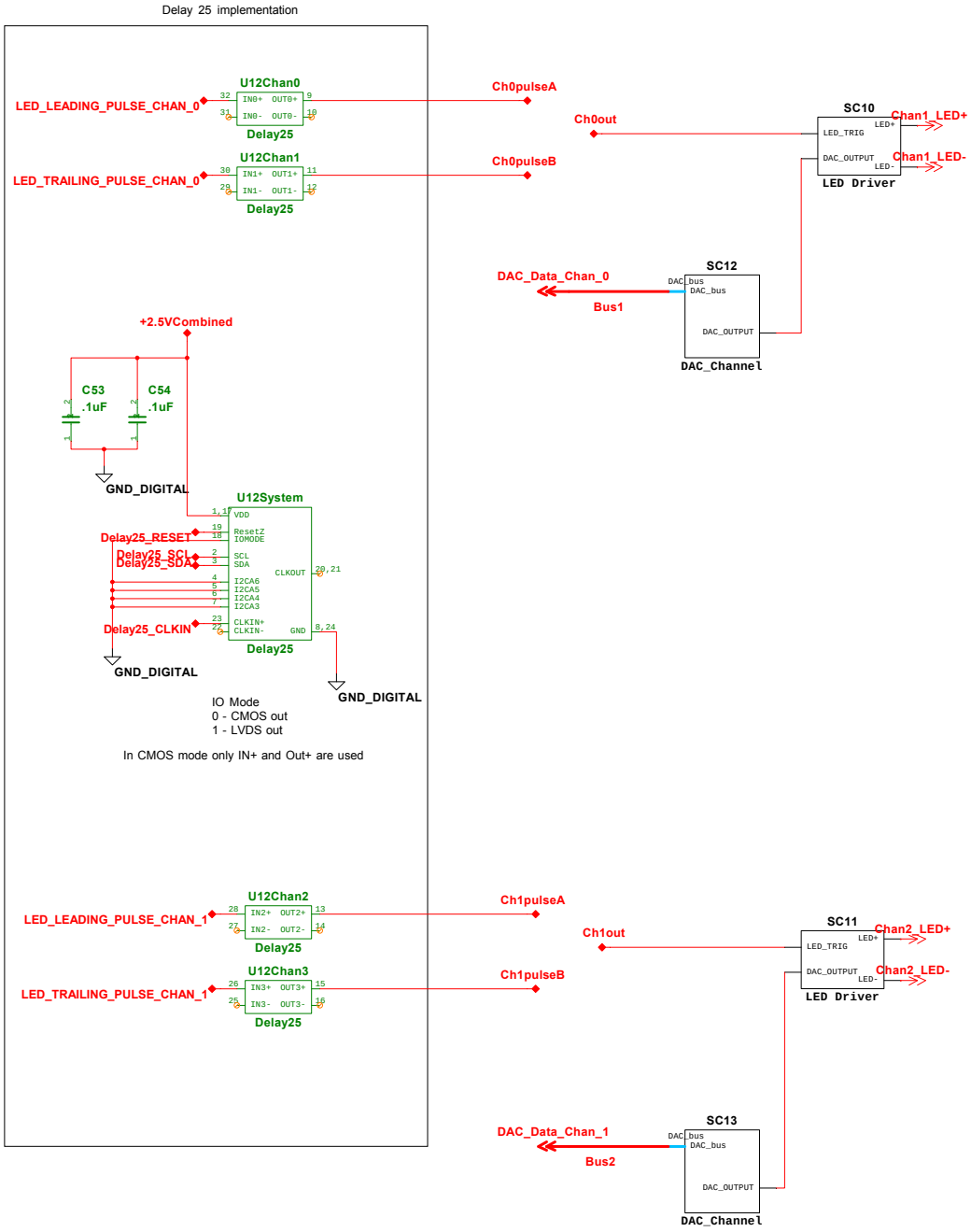

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Project Name:	HE Pulser Rev2_2#Delay25
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Page Description:	HE Pulser Rev2_2
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Project Code:	
Rev:	2.2
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Approved:	
CAGE Code:	4B817
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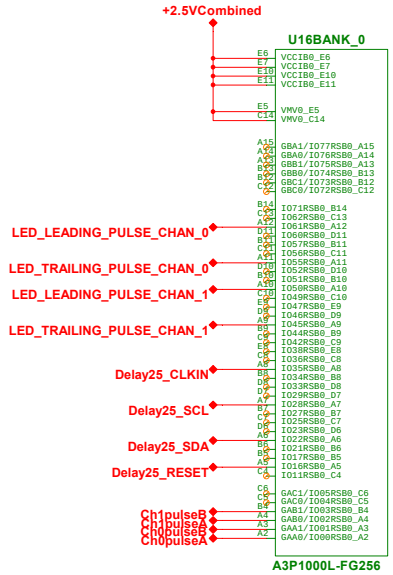
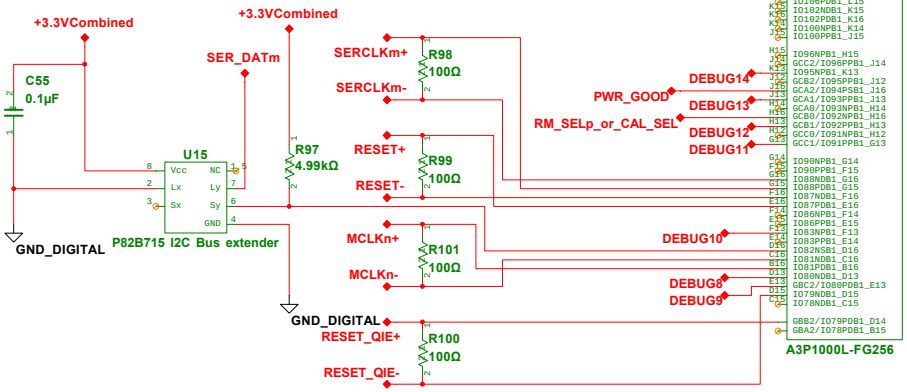
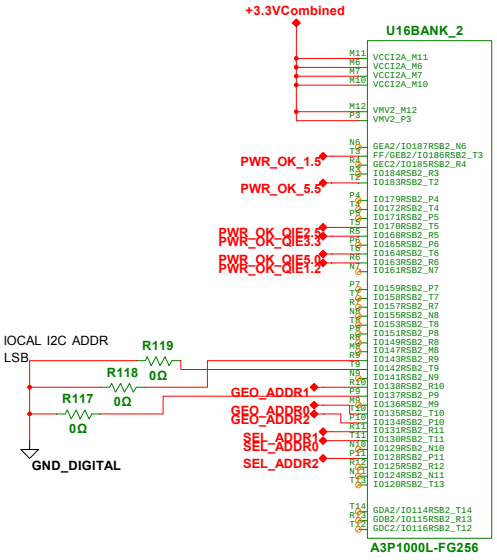
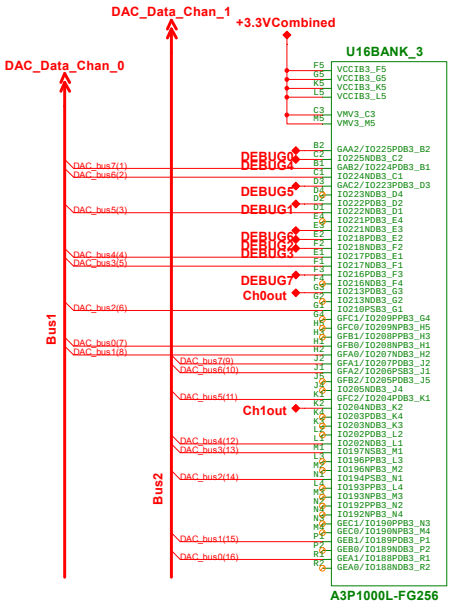
Sheet:	4 of 13

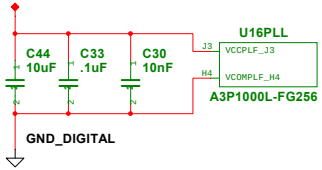
Bank 0 used for interface with the Delay25 chip which is 2.5V CMOS.
This bank's I/O Standard is LVCMOS 2.5/5.0 V. This standard is similar to LVCMOS 2.5 V,
with the exception that it can support up to 3.3 V on the input side (2.5 V output drive).











Incorrect symbol. Pin is on Bank 1

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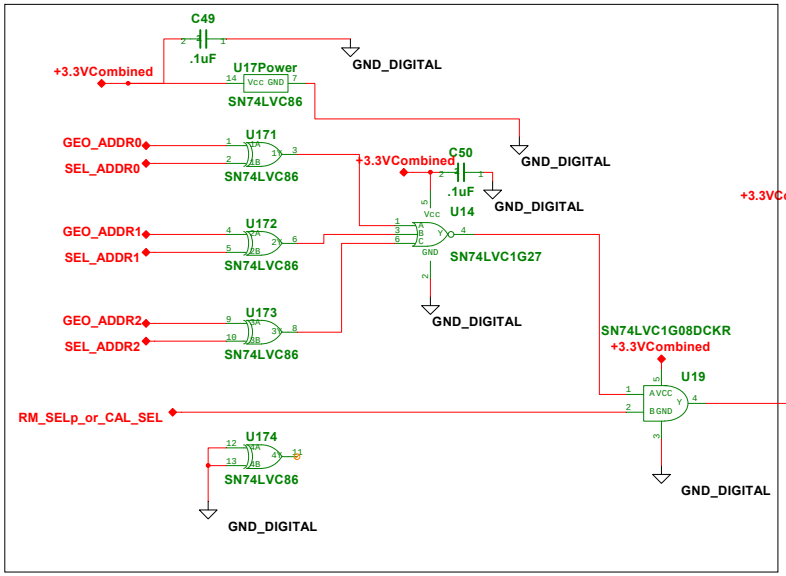
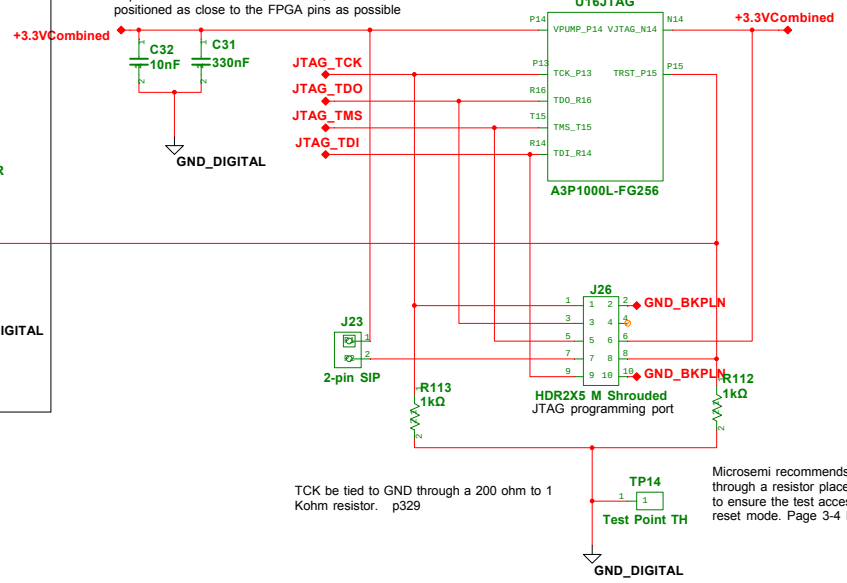
Approved:	CAGE Code: 4B817	Date: 10/28/2015	Sheet: 5 of 13

Backplane JTAG address decoding



ProASIC3L Fabric Guide Page 337
For proper programming, 0.01 µF and 0.33µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible

JTAG header information
Page 335 ProASIC3L
Fabric user guide



TCK be tied to GND through a 200 ohm to 1 Kohm resistor. p329

Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin to ensure the test access port (TAP) is held in reset mode. Page 3-4 PA3L_DS.pdf

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Revision 1

Sergey V Los version

Revision 2.0 July 2015

EDL prototype released July 2 2015

Revision 2.1

Added 0154005.DR Fuse inbetween V1 and the backplane connector J12.
Removed ferrite beads from Pin Diode connections.
Replaced Power Enable logic gates with Rad-Hard MOSFET BST82215.
Removed the logic gate for Igloo-enable.
Removed ferrite beads from Pulser Power Regulator outputs.
Connected vsense (pin 14 documented as NC) to Vout (pins 15, 16) on regulator circuits.
Changed Bank_0 to +2.5v.
Changed Bank_2 to +3.3v.
Replaced 3-input AND on GEO/SEL_ADDRESS's decoding to SN74LVC1G27 3-input NOR.
Made extra page for documenting changes. (This page)
Replaced SN74LVC1G08DCKR 2-input AND gates with on-chip logic on FPGA.
Changed the pin for Debug1-4, and for the two AND gates.
Changed R97 on I2C buffer from 100k to 5k
Corrected Symbol pin error on FPGA where Bank2 contained D14 and B15 from Bank1

Revision 2.2 DC-DC converters. October 2015

Combined power supplies from 9 LHC4913s to
    2 LHC4913 and
    4 FEASTMP_CLP DC-DC converters
Added EDL label
Added to project Daughter board LMZ31704 DC-DC converter to standin for the
    FEASTMP_CLP until it becomes available in December
Removed connections to QIE V1 on connector J4

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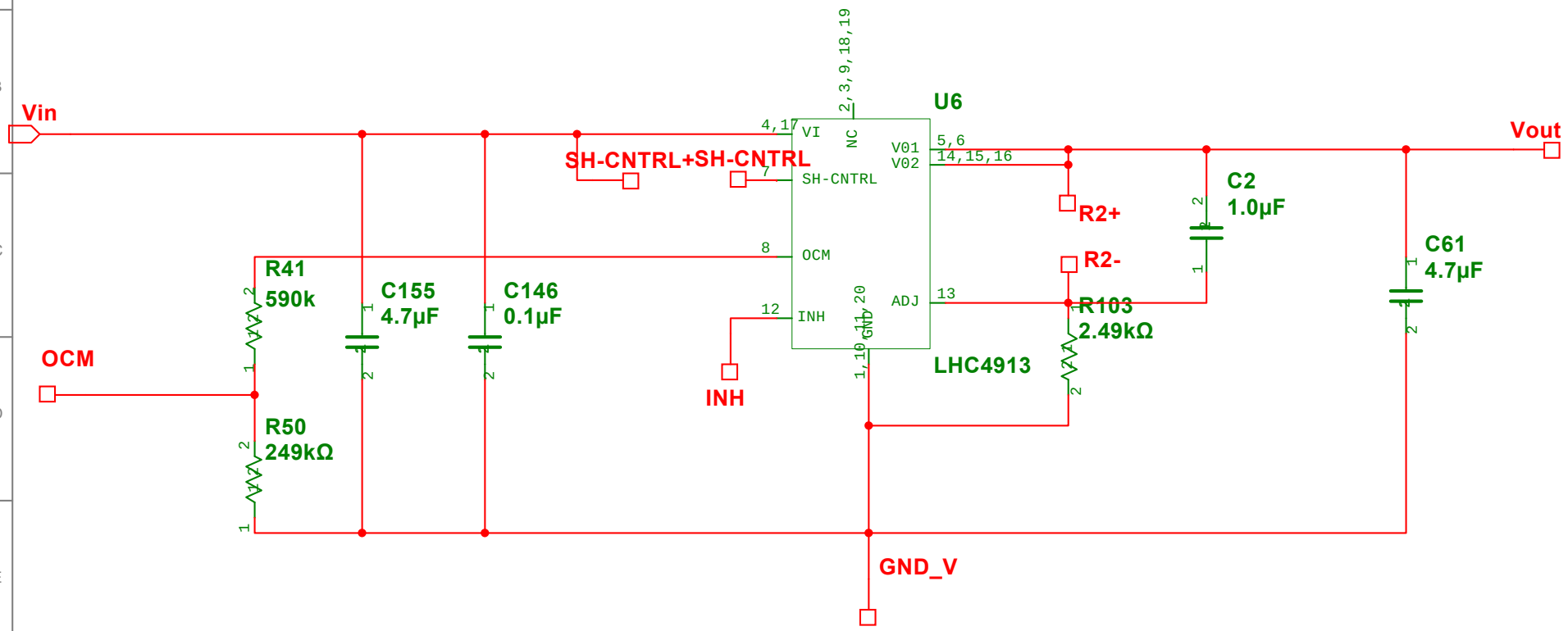
Checked By:	Page Description: HE Pulser Rev2_2			
	Project Code:		Rev: 2.2	Size: C
Approved:	CAGE Code: 4B817	Date: 10/28/2015	Sheet: 7 of 13	



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Project Name: LHC4913_Circuit(SC1)

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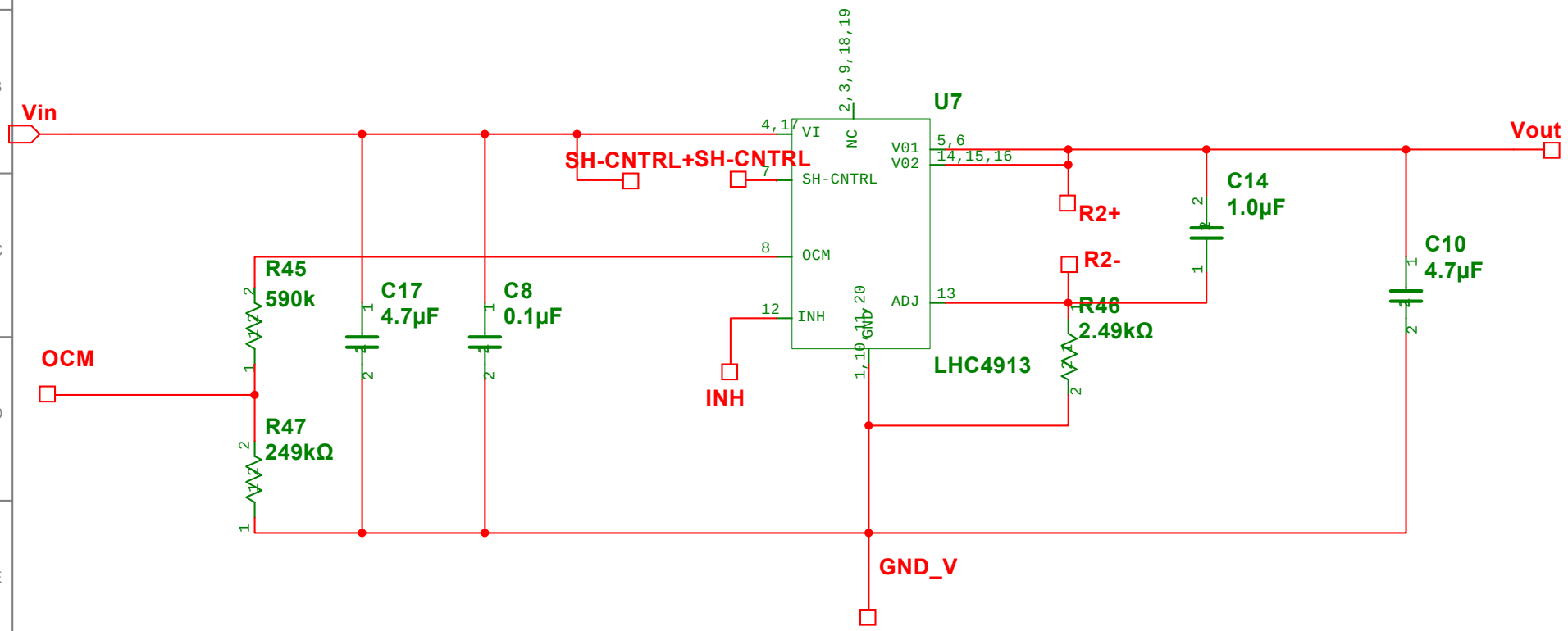

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Project Name: LHC4913_Circuit(SC2)				
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Checked By:	Project Code:		Rev: 2.2	Size: C
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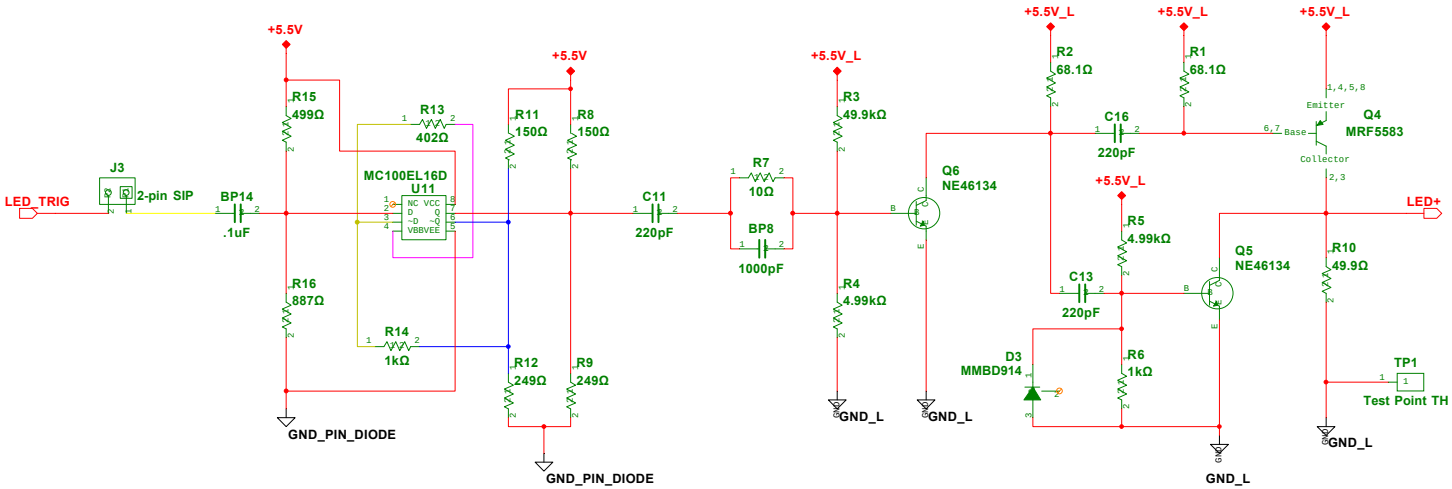

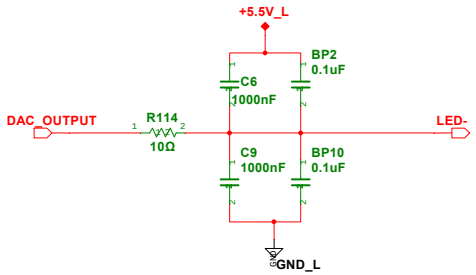

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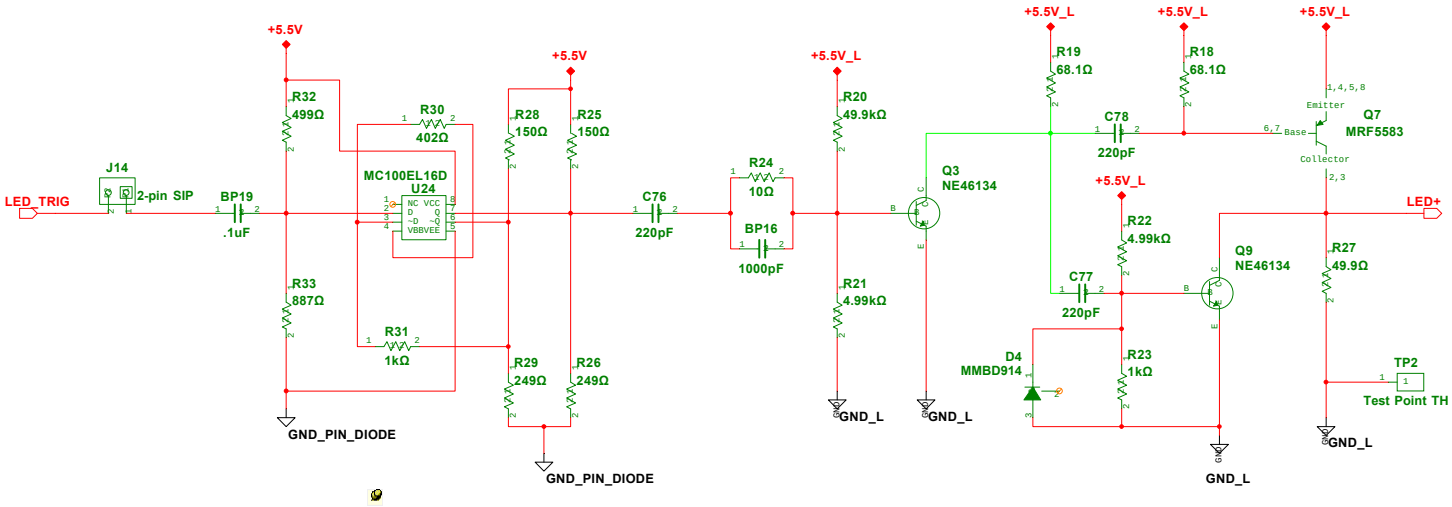
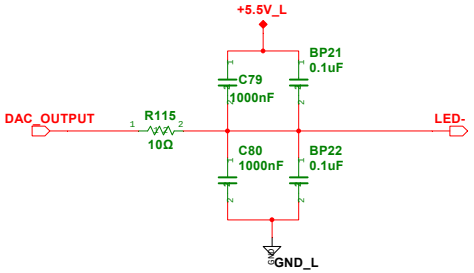
Checked By:	Project Code:	Rev:	Size: C
Approved:	CAGE Code: 4B817	Date: 10/28/2015	Sheet: 10 of 13





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Checked By:	Page Description: HE Pulser Rev2_2	Rev:	Size: C
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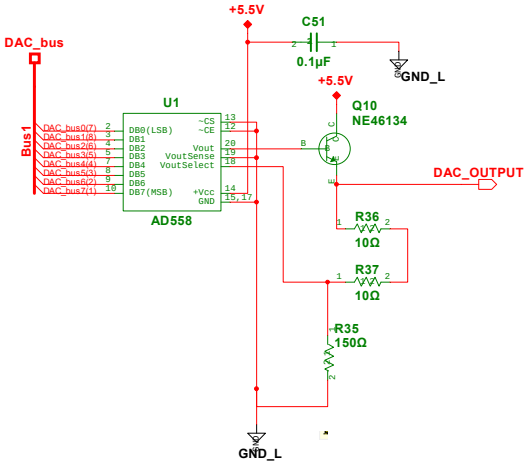
	CAGE Code: 4B817	Date: 10/28/2015	Sheet: 11 of 13



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Project Code:	
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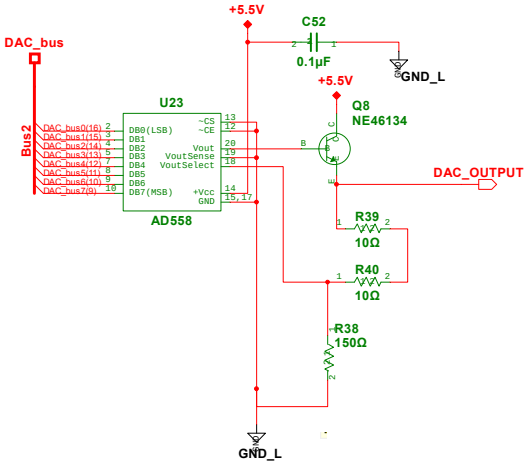
Sheet:	12 of 13



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CAGE Code:	4B817
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Sheet:	13 of 13