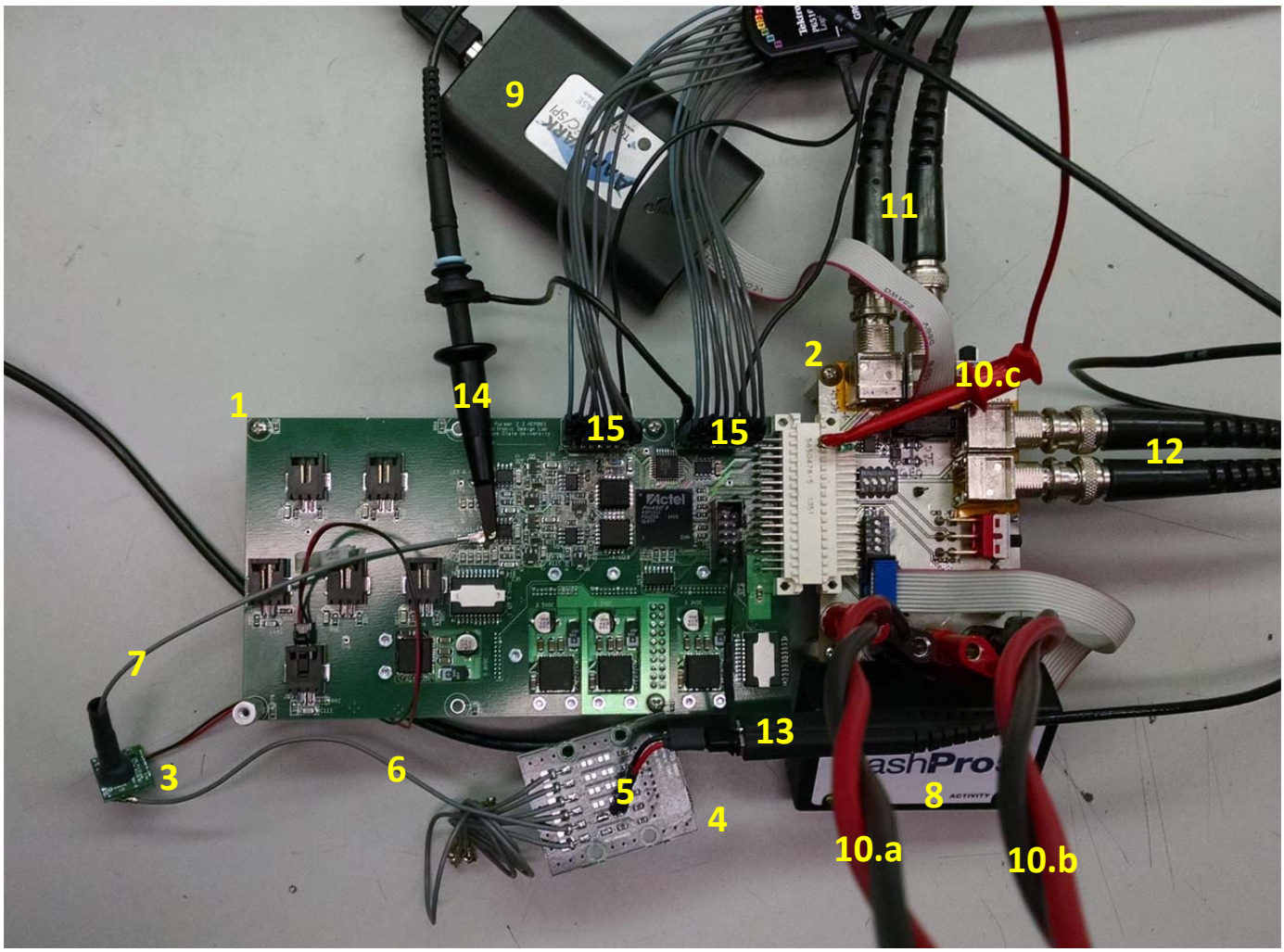
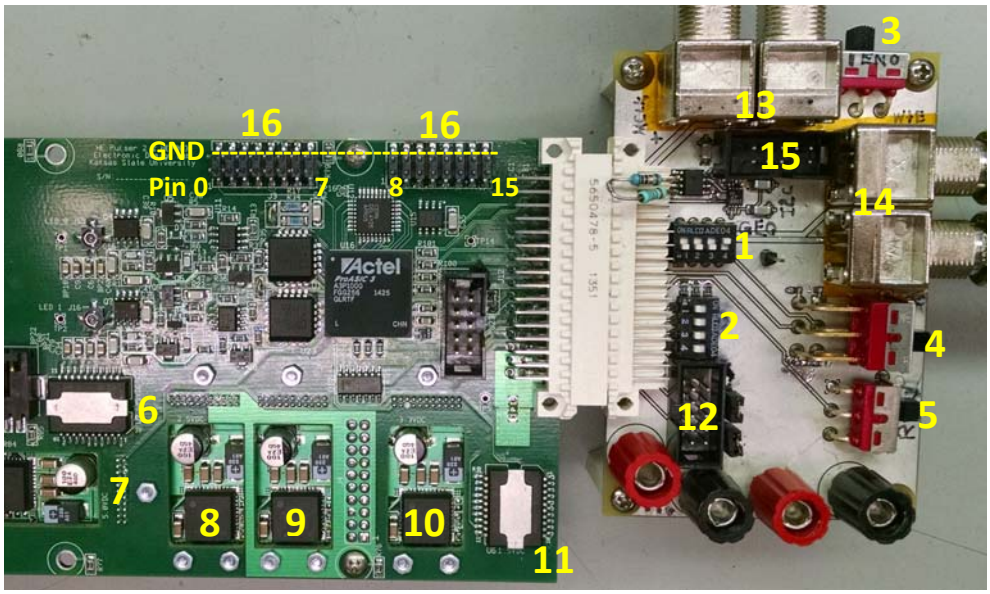
# 7. HE Pulser test specification

## 7.1. Hardware test setup

1. HE Pulser board (Device Under Test DUT)
2. Backplane simulator
3. Pin diode board
4. QIE11 Adapter board (showing Rev1.0)
5. 50Ω terminating resistor
6. Pin Diode board to QIE11 Adapter board Coaxial cable
7. NSPG320BS LED assembly
8. FlashPro5 FPGA programmer
9. Aardvark $I^2C$/SPI communication tool or equivalent
10. Three output power supply:
    a) 11VDC @ 0.2A
    b) 3.3VDC @ 0.1A
    c) 1.8VDC @ 0.05V
11. MCLK clock pulse generator
12. WTE pulse generator
13. Oscilloscope with differential probe input
14. LED output pulse probe (not required)
15. Debug outputs (optional)



## 7.2. Initial settings and Test 1: Power up function tests




Set switch positions

1. GEO_ADDR = 0001
2. SEL_ADDR = 0000
3. PWR_ENABLE on (left on)
4. RESET off (Down off)
5. RM_SEL on (up on)

Power on the backplane 11VDC, 3.3VDC, 1.8VDC

6. Verify 5.5VDC (pin 14,15,16)
7. Verify 5VDC (Pin 11 bottom right)
8. Verify 2.5VDC (Pin 11 top right)
9. Verify 1.2VDC (Pin 11 top right)
10. Verify 3.3VDC (Pin 11 top right)
11. Verify 1.5VDC (pin 14,15,16)
12. JTAG program FPGA using the latest firmware
13. Enable MCLK (40MHz LVPECL)
14. Enable WTE (100Hz 25ns pulse LVPECL sync to MCLK)
15. $I^2C$ Write, and verify with read, hex value `03 00 03 00 03 00 00 00 FF 00 FF` (Target power must be enabled in Aardvark GUI menu option, Slave address 0x30, read/write 11 bytes)
16. Using Debug Header verify
    - Reset signal (Pin 1) matches RESET switch (Down off, Up On)
    - PWR_GOOD signal (Pin 7, backplane pin A7) is asserted if all voltage levels are correct as measured in 6-11
    - Verify Pin 0 matches MCLK clock input
    - Enable WTE input signal and verify Pin 2 matches WTE input

## 7.3. Test 2: $I^2C$ communications

Write then read a malformed $I^2C$ message and ensure communication continues. Transmit then read the following commands and ensure the output pulse is correctly modified on the last transmit:

- `03 00 03 00 03 00 00 00 80 00 80`
- `03 FF FF FF FF 00 00 00 FF 00` (R/W 10 bytes)
- `03 FF FF FF FF 00 00 00 FF 00 FF FF` (R/W 12 bytes)
- `03 00 03 00 03 00 00 00 FF 00 FF` (R/W 11 bytes)

Add to the oscilloscope traces WTE. Verify the WTE correctly places the output pulse with respect to the bunch count setting.

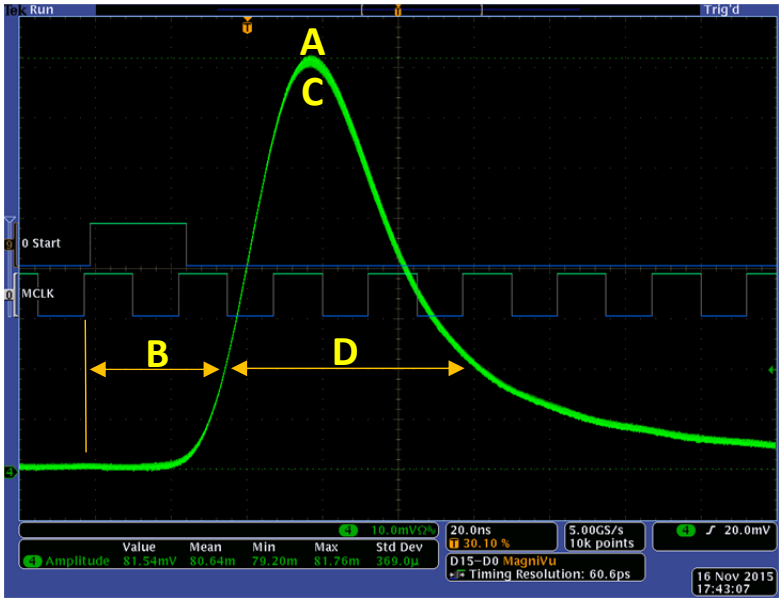
- `03 00 03 00 03 00 00 00 FF 00 FF` gives 3 MCLK counts before pulse start
- `03 00 0F 00 0F 00 00 00 FF 00 FF` gives 15 MCLK counts before pulse start
- `03 FF FF FF FF 00 00 00 FF 00 FF` gives maximum MCLK delay

## 7.4. Test 3: LED Pulser Signal at Different DAC Settings

On the testing oscilloscope, trace the differential output from the 50Ω termination resistor using 10s persistence and the trigger set to 25% of the pulse peak voltage (e.g. 20mV). Observe MCLK signal and the LED start pulse (debug pin 9).

The Trigger signal is the MCLK rising edge preceding the start pulse (debug pin 9).

For each of the $I^2C$ settings below measure the values for the tabulated plot elements. Verify measurements lie within values by ±10mv or ±10ns




| Hex $I^2C$ message (Slave address 0x30) | Description | Pulse average peak voltage (mV) (A) | Trigger to 25% Pulse average peak voltage (ns) (B) | Pulse peak time (ns) (C) | Pulse width at 25% Pulse peak voltage (D) |
|---|---|---|---|---|---|
| 03 00 03 00 03 00 00 00 FF 00 FF | Max amplitude, no delay, max width | 80mV | 37ns | 60ns | 65ns |
| 03 00 03 00 03 40 40 00 FF 00 FF | Middle amplitude, no delay, max width | 41mV | 40ns | 62ns | 69.4 |
| 03 00 03 00 03 00 00 19 FF 19 FF | Max amplitude, middle delay, max width | 78mV | 49.8ns | 71ns | 65ns |
| 03 00 03 00 03 00 00 32 FF 32 FF | Max amplitude, max delay, max width | 78mV | 62ns | 85ns | 65ns |
| 03 00 03 00 03 00 00 00 80 00 80 | Max amplitude, no delay, middle width | 77mV | 62ns | 85ns | 65ns |