For review purposes only – not finalized for design use

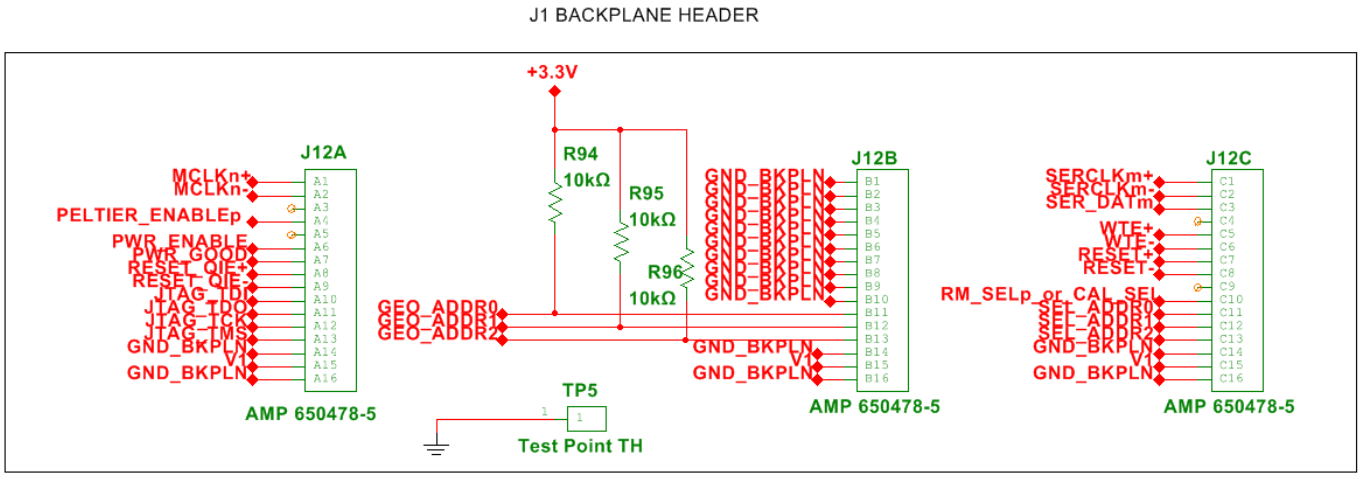
2. HE Pulser Rev 2.2 Datasheet

2.1. Description

As part of the HCAL upgrade Phase I, The HE Pulser now offers improved programmable control over the LED pulse to the QIE calibration scintillator. The LED pulse may be positioned between 2 and 65,535 MCLK counts from a resetting WTE signal. This pulse can be delayed from the triggering MCLK signal from 0 to 25ns in 0.5ns increments. The pulse amplitude and width is programmable from ~85mV to ~4.75V and 0.5ns to 25ns respectively. It also provides power for the 6 pin diodes and the QIE 11 PCB.

The HE Pulser Rev 2.2 receives communication and clock synchronization (MCLK) from the ngCCM through the backplane header. The LED output is

2.2. Backplane header (AMP 650478-5)



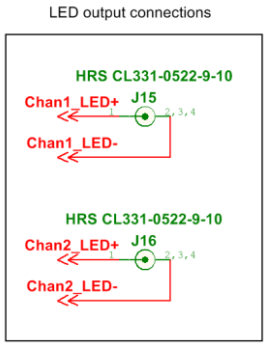
Signal	Level	Definition
MCLKn±	LVPECL input	40 MHz free running ncCCM clock
Peltier_Enable		Not used
PWR_ENABLE	LVTTL input	Active high backplane signal assuring the V1 power source is stable.
PWR_Good	LVTTL Output	Active high when Power regulators are functioning normally.
Reset_QIE		Not used
JTAG (4 signals)		Programming access to Microsemi A3P1000L FPGA.
V1	11 VDC input	Primary input voltage. Onboard 3Amps fuse.
GEO_ADDR0,1,2	Float or ground	Identifies the physical address of the backplane connection.
SERCLK ±	LVPECL input	I2C communication clock
SER_DAT	Bi-directional	I2C communication data signal.
WTE ±	LVPECL input	Bunch counter reset
Reset ±	LVPECL input	Reset to power on state
RM_SEL or CAL_SEL	LVPECL input	Active high indicates JTAG programming is active
SEL_ADDR0,1,2	LVTTL input	Matches the GEO_ADDR for JTAG programming

2.3. LED pulse outputs, LED channel 0 and 1

The two LED outputs are provided on two Hirose connectors located near the center of the PCB. Jumpers J3 and J14 disconnect the digital pulse generator from the analog portion allowing individual testing or excitation.

DAC Outputs change to LED pulse output voltages

Pulse Amplitude register (DAC setting)	LED pulse voltage (V)
00	0.84
32	1.51
64	2.33
96	3.11
C8	3.89
EB	4.45
FF	4.75

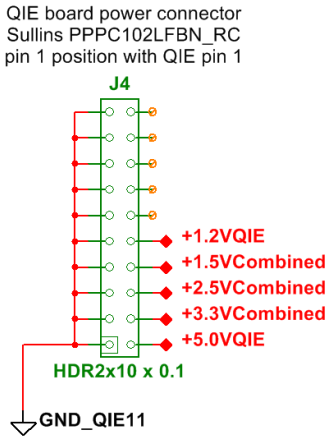


2.4. Pin Diode power supply outputs J

The HE Pulser board offers six TE Connectivity AMP 147323-1 connectors providing a total of 0.75A at 5.5Vdc (Pin 1) and Ground (Pin 2) for powering Pin Diodes.

2.5. QIE11 power header J4 (Sullins PPPC102LFBN_RC)

Five voltage supplies are provided for driving the QIE11 through the J4 inter-board connecting header. J4 is positioned to align with QIE11 J1. It is required that the Samtec IPT1-110-01-L-D-RA 90° header be removed and replaced with Samtec MTSW-110-xx-L-D-xxx header.



2.6. I²C communication

The backplane is an "I2C – like" serial interface. It consists of a clock line (SER_CLK) implemented as differential LVPECL with pulldown resistors on the ngCCM and 100 ohm differential termination on the HE Pulser Board. The data line is open drain (SER_DAT). The ngCCM is the master. The data line is an open drain line to be pulled up by the ngCCM.

The HE Pulser board address is 0x30. The I²C message must read or write all 11bytes in the following format:

HE Pulser Rev 2.2 I²C communication protocol		
Byte	**Usage**	**Range**
1	Command byte	See Command Byte bit map
2	Bunch Count Register Channel 0 MSB	0 to FF FF. The number of MCLKs to be counted before sending the Channel 0 LED pulse
3	Bunch Count Register Channel 0 LSB	
4	Bunch Count Register Channel 1 MSB	0 to FF FF. The number of MCLKs to be counted before sending the Channel 1 LED pulse
5	Bunch Count Register Channel 1 LSB	
6	Pulse Amplitude Channel 0	0 (maximum pulse) to 255 (minimum pulse).
7	Pulse Amplitude Channel 1	0 (maximum pulse) to 255 (minimum pulse).
8	LED Pulse Delay Channel 0	0 to 50 (0x32) for a width of 0.0 to 25 ns. Value of 12 (0x0C) times to next MCLK.
9	LED Pulse Width Channel 0	0 (minimum width) to 255 (maximum width)
10	LED Pulse Delay Channel 1	0 to 50 (0x32) for a width of 0.0 to 25 ns. Value of 12 (0x0C) times to next MCLK.
11	LED Pulse Width Channel 1	0 (minimum width) to 255 (maximum width)

Command byte format		
Bit position	**Value**	**Command**
MSB bit 7	X	Unused
Bit 6		
Bit 5		
Bits [4:2]		Debug register. Select debug output signals
Bit 1		Active high LED 1 Enable
Bit 0		Active high LED 0 Enable