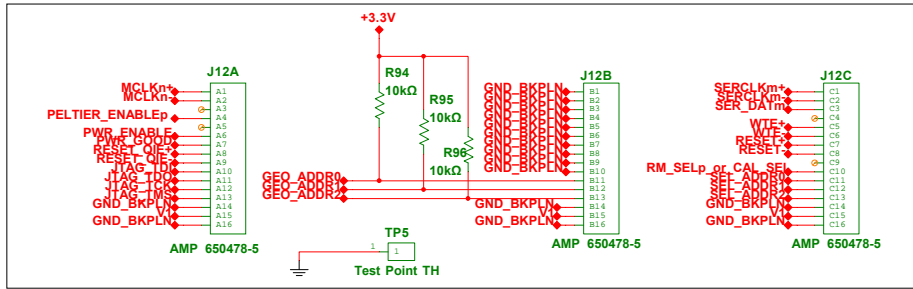
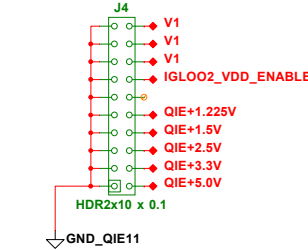


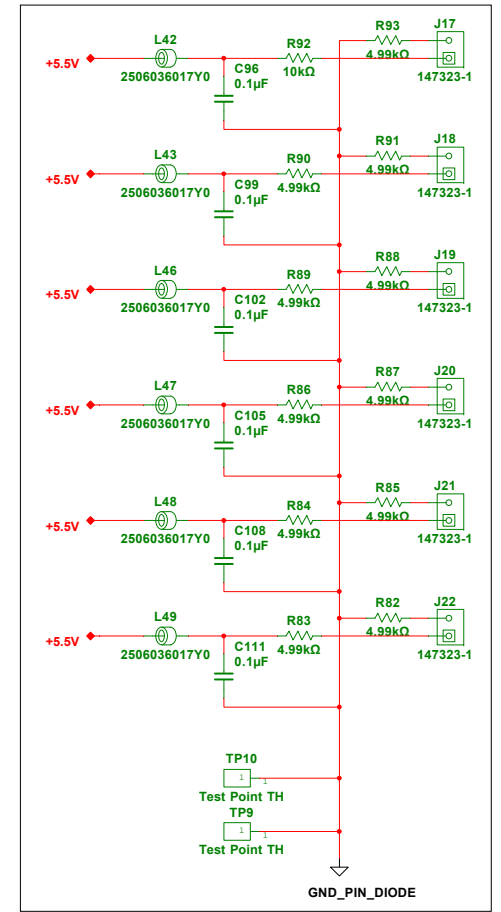
J1 BACKPLANE HEADER



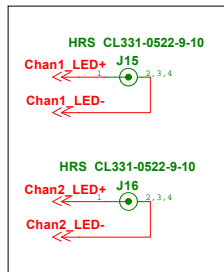
QIE board power connector
Do not populate
verify pin 1 position with QIE position



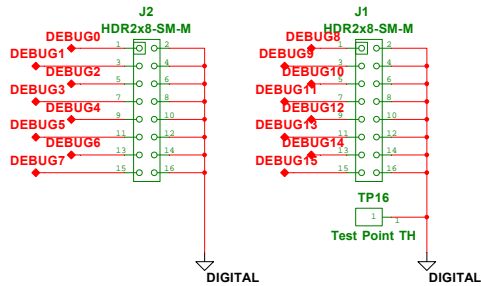
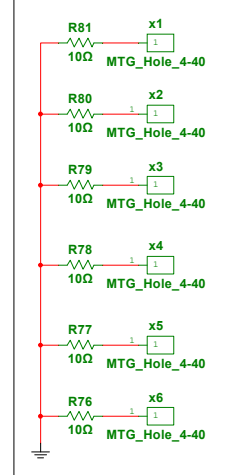
Pin Diode connections



LED output connections

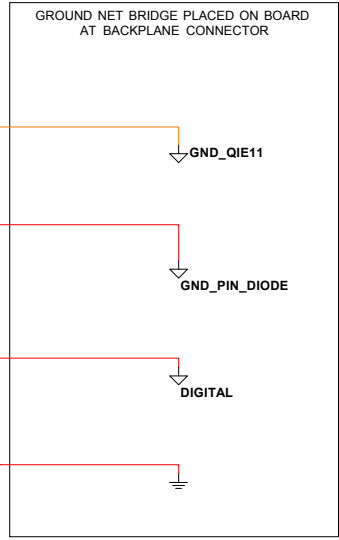
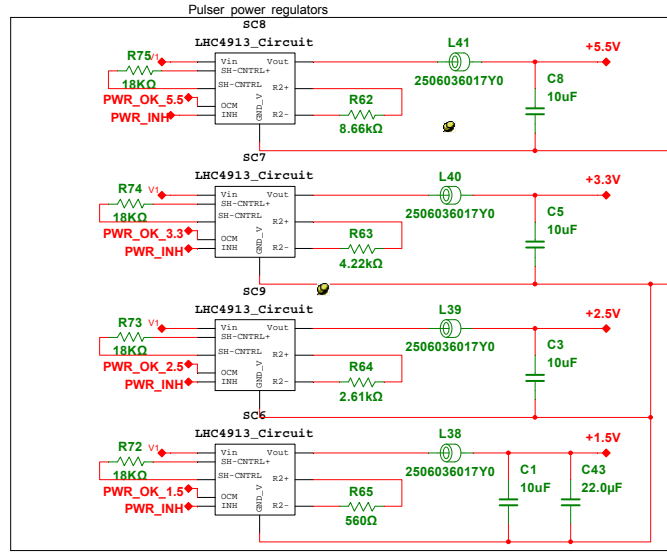
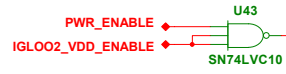
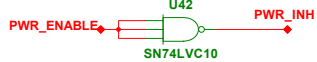
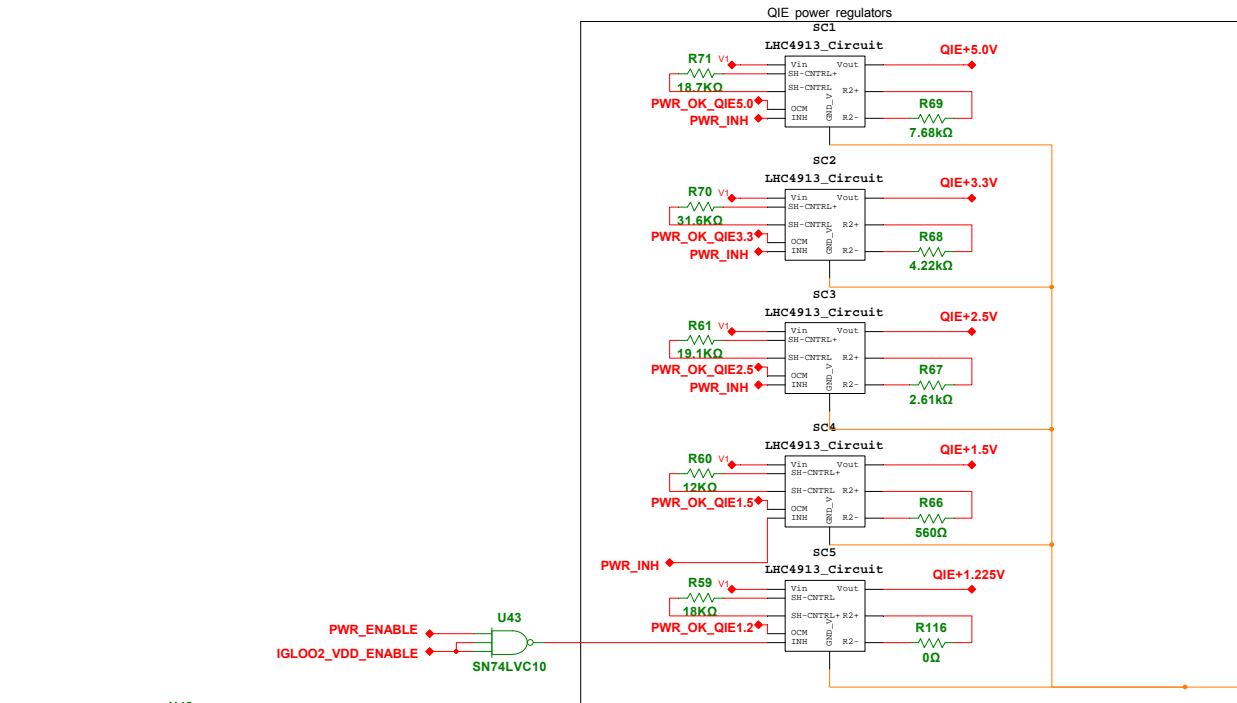


Board mounting holes



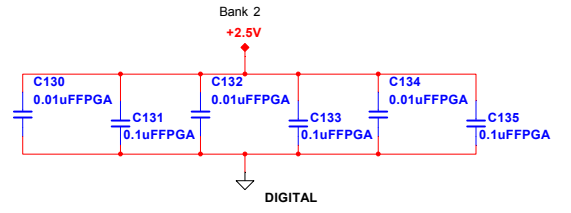
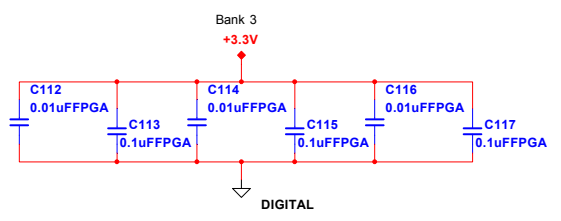
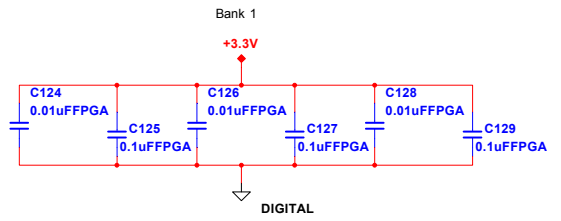
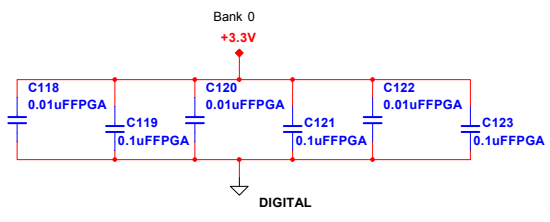
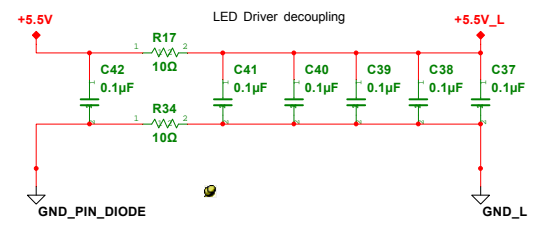
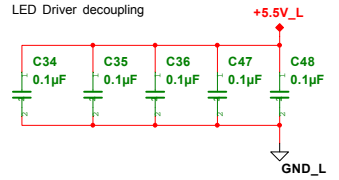
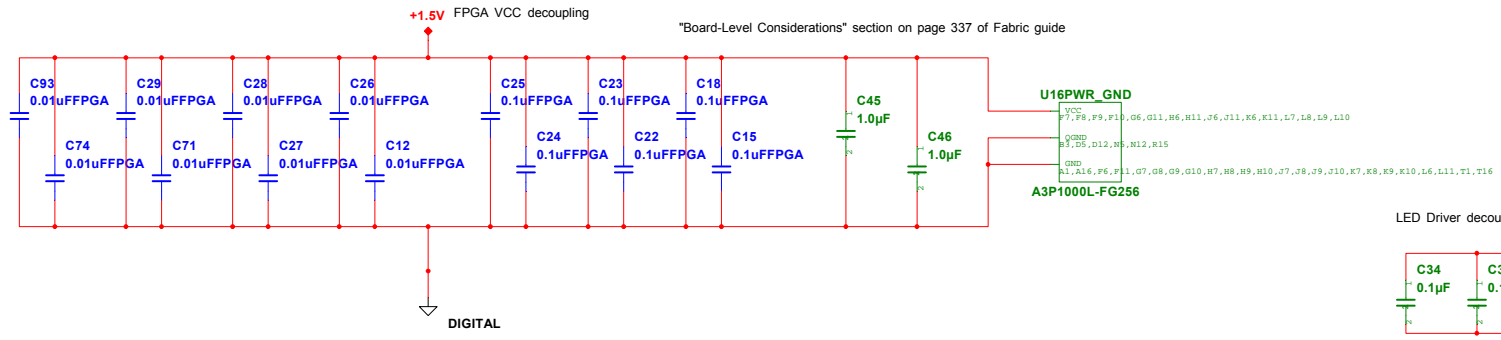
EDL Electronics Design Laboratory	Electronics Design Laboratory 124 Burt Hall Kansas State University Manhattan, KS 66506 785-532-7826		
	Project Name: HE Pulser Rev2#External connections		
Designer: © 2013, SCorkill Checked By:	Page Description: HE Pulser Rev2 Project Code: HEP083 CAGE Code: 4B817	Rev: 2 Date: 8/20/2015	Size: C Sheet: 1 of 19

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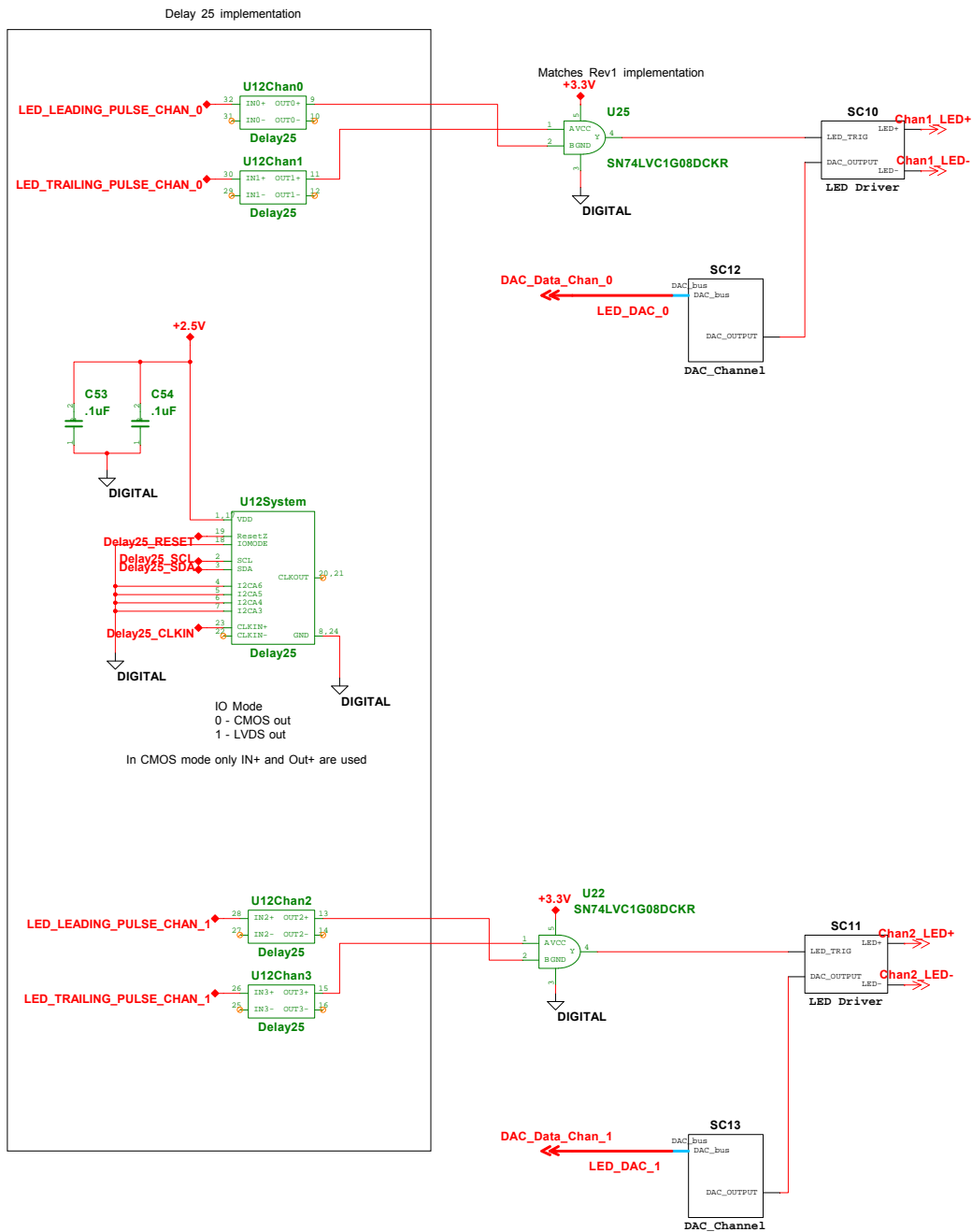
EDL Electronics Design Laboratory	Electronics Design Laboratory		
	124 Burt Hall Kansas State University Manhattan, KS 66506 785-532-7826		
Designer:	Project Name: HE Pulsar Rev2#Power systems		
Checked By:	Page Description: HE Pulsar Rev2		
Approved:	Project Code: HEP083	Rev: 2	Size: C
	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 2 of 19

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Designer: © 2013,	Page Description: HE Pulser Rev2			Rev: C
Checked By:	Project Code:	Date: 8/20/2015	Sheet: 3 of 19	Approved:

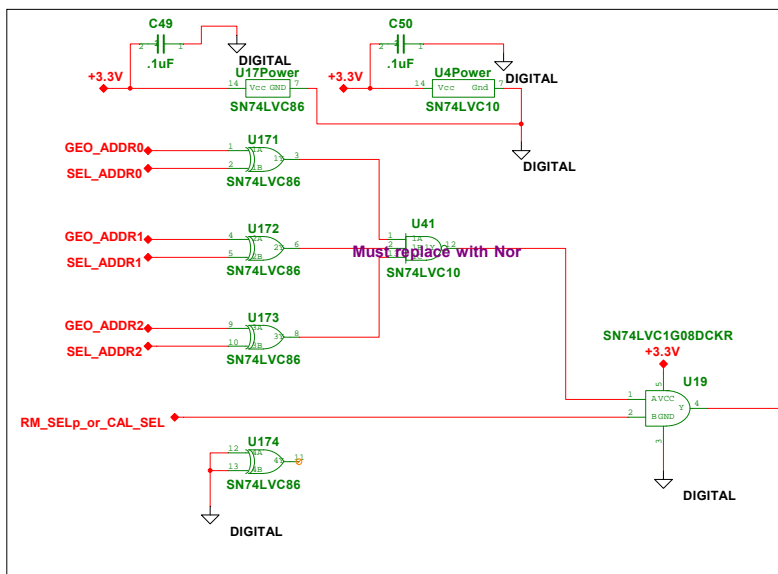
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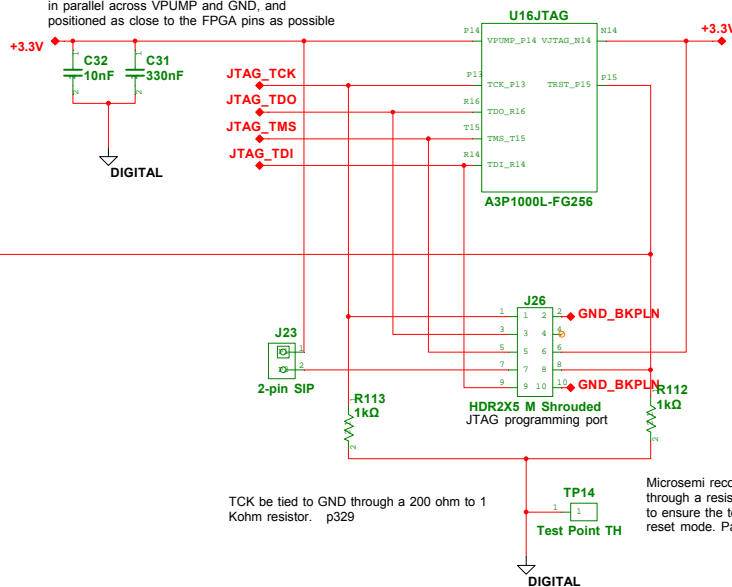
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Designer: © 2013, Checked By:	Project Code: 4B817	Rev: 4	Size: C
Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 4 of 19

Backplane JTAG address decoding



ProASIC3L Fabric Guide Page 337
 For proper programming, 0.01 μF and 0.33 μF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible

JTAG header information
 Page 335 ProASIC3L
 Fabric user guide

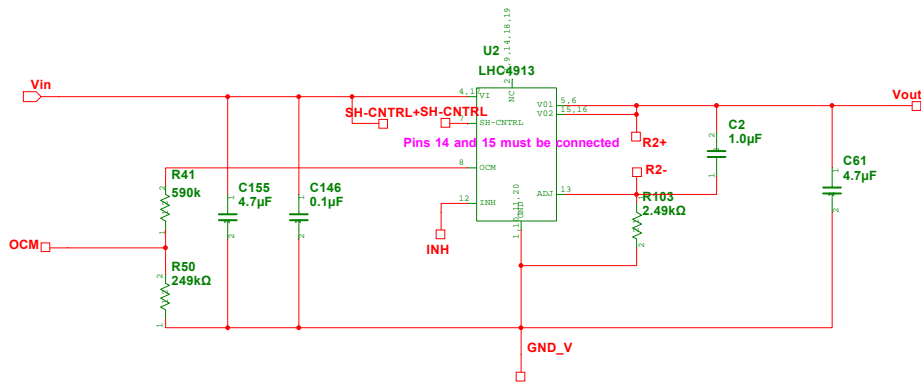


TCK be tied to GND through a 200 ohm to 1 Kohm resistor. p329


Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin to ensure the test access port (TAP) is held in reset mode. Page 3-4 PA3L_DS.pdf

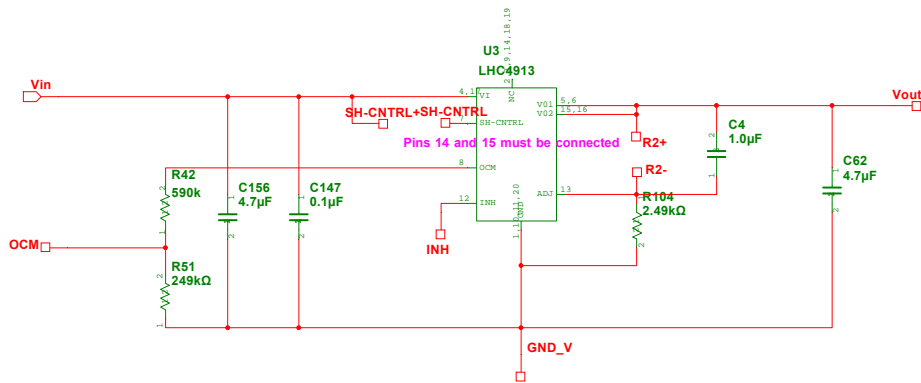
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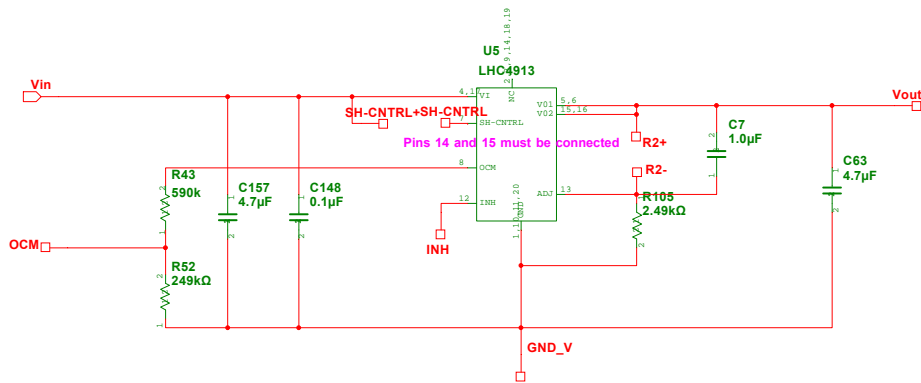
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	Project Name: LHC4913_Circuit(SC1)			
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Checked By:	Project Code:	Rev:	Size: C	
Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 7	of 19



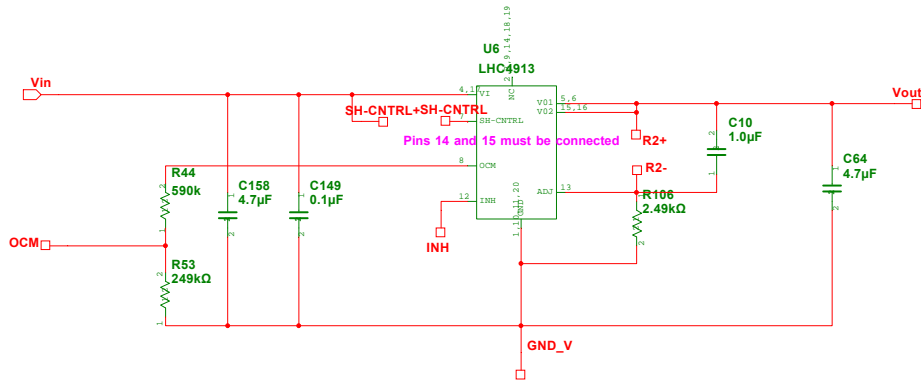
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 8	of 19




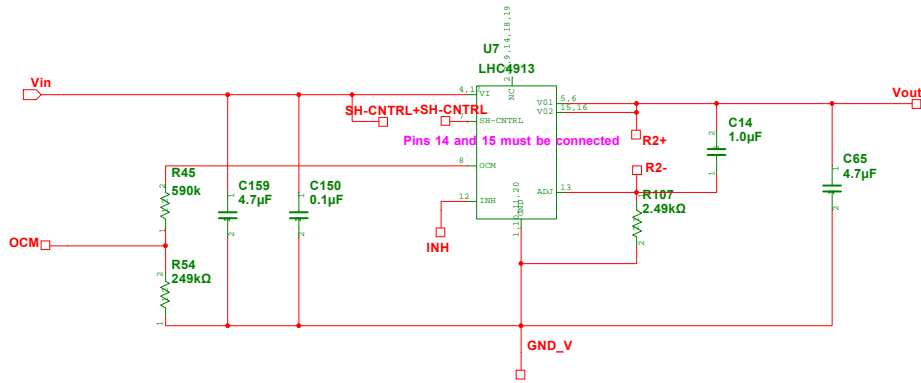
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 9	of 19



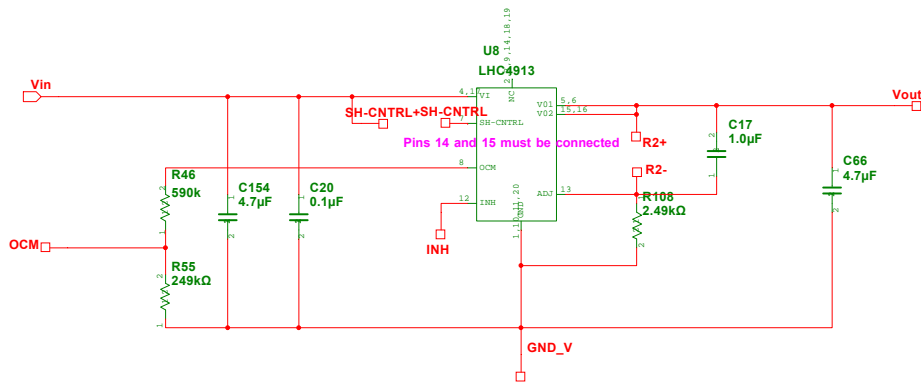
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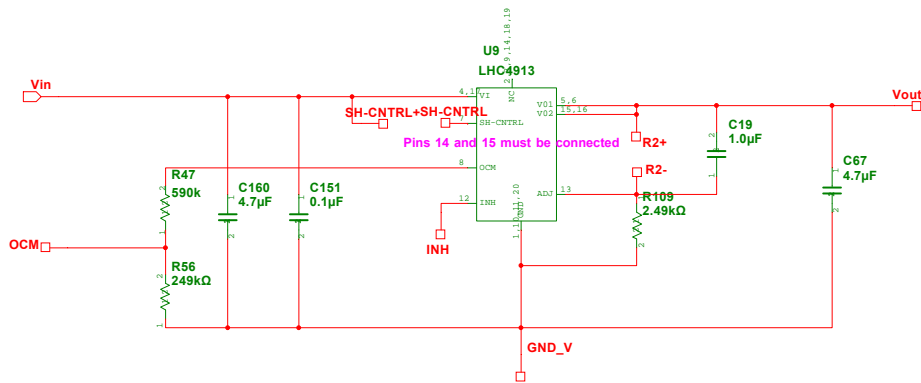
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Checked By:	Project Code:	Rev:	Size: C	
Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 11	of 19




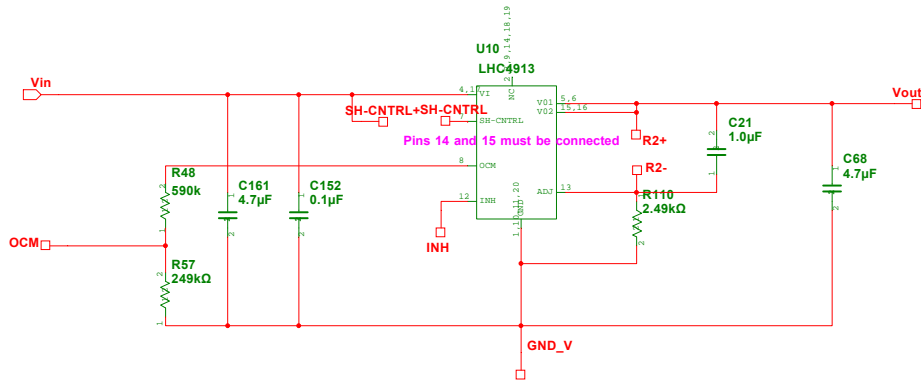
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 12 of 19




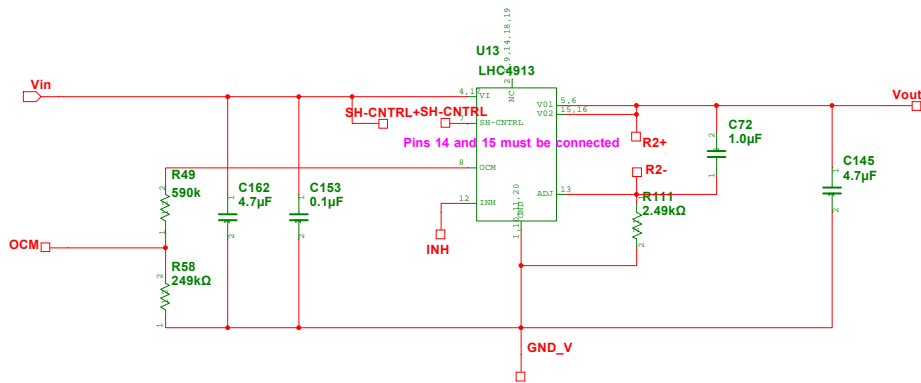
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Designer: © 2013,	Page Description: HE Pulser Rev2			
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 13	of 19




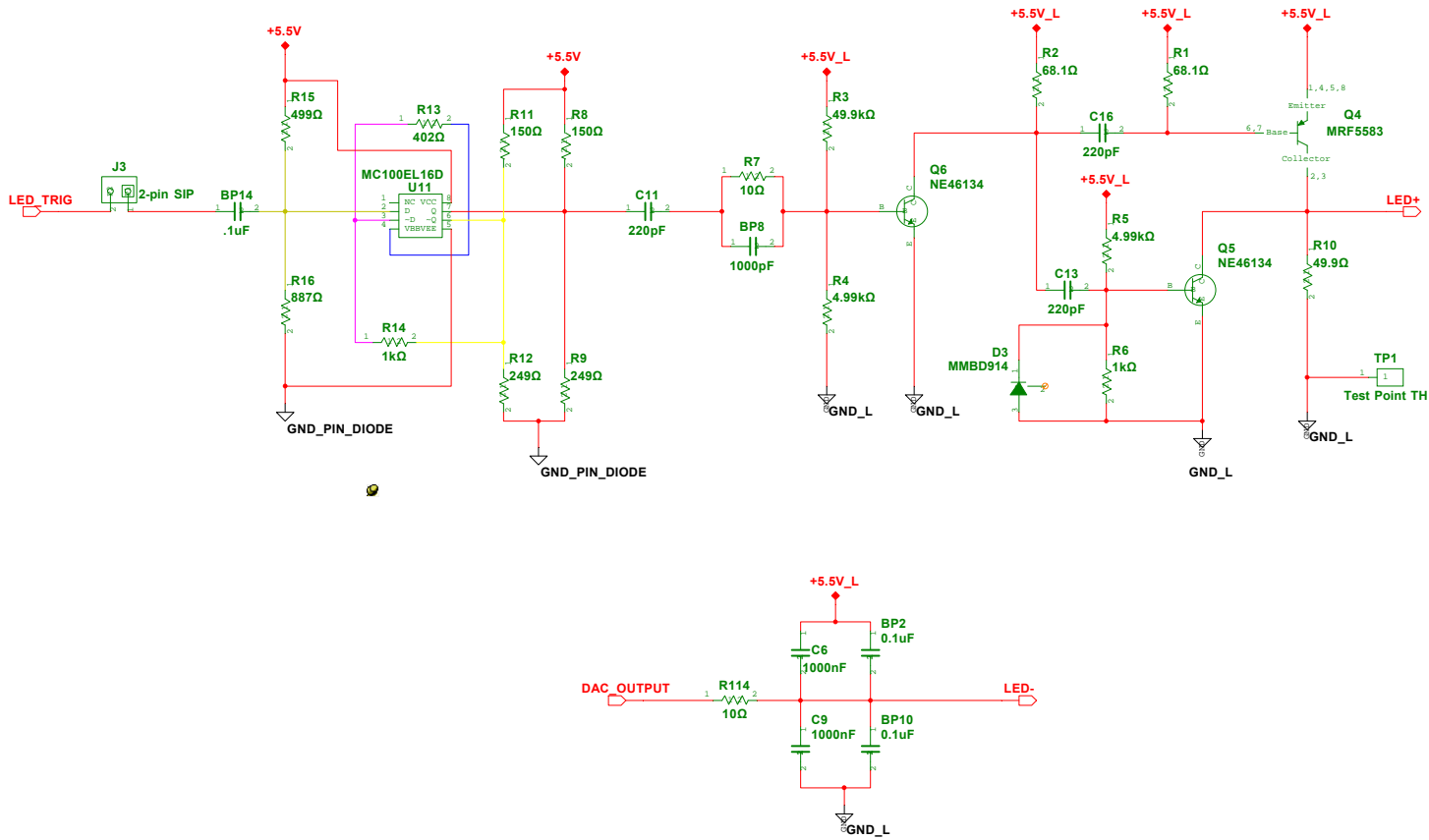
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	Project Name: LHC4913_Circuit(SC8)			
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 14 of 19	Size: C




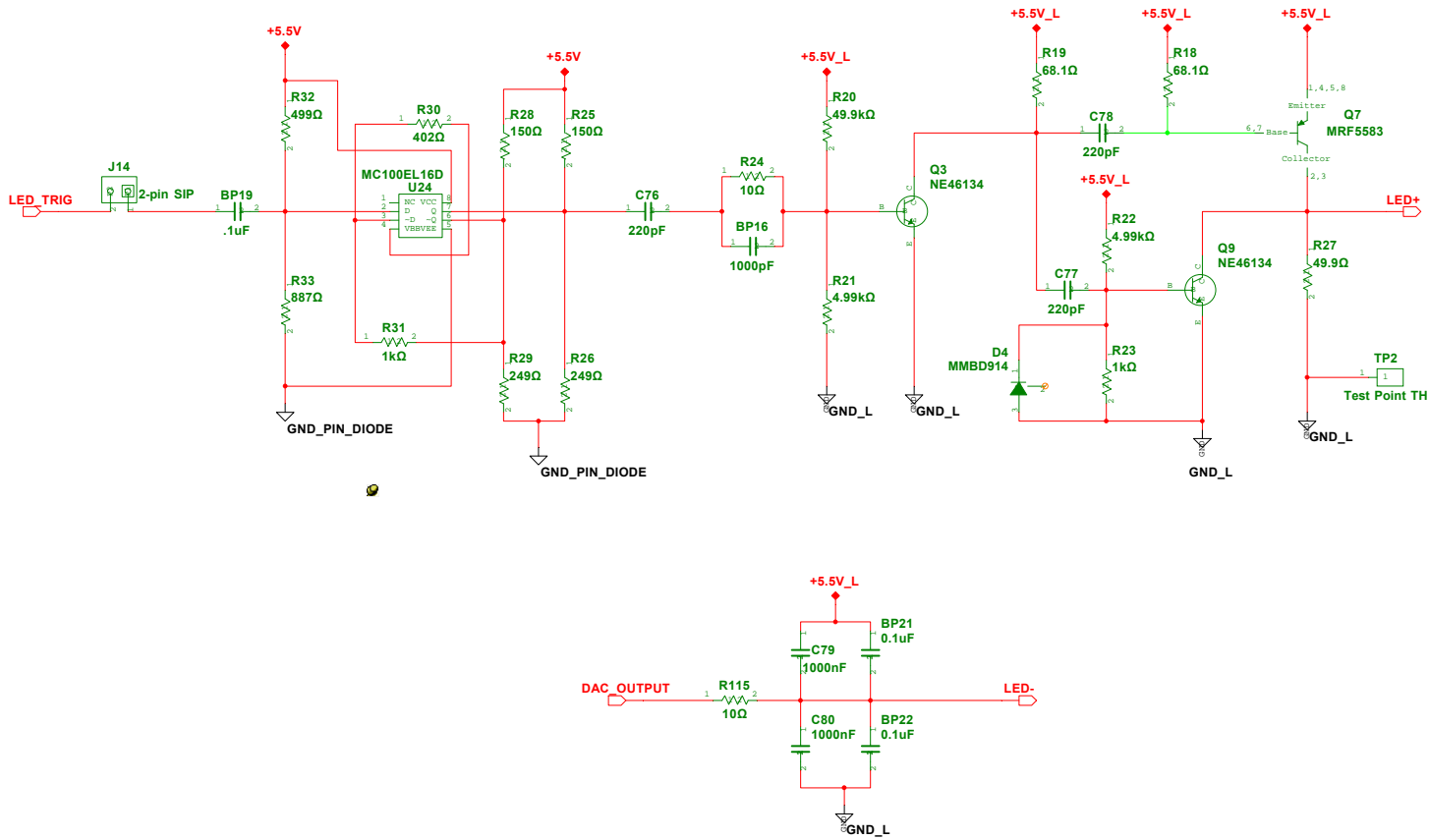
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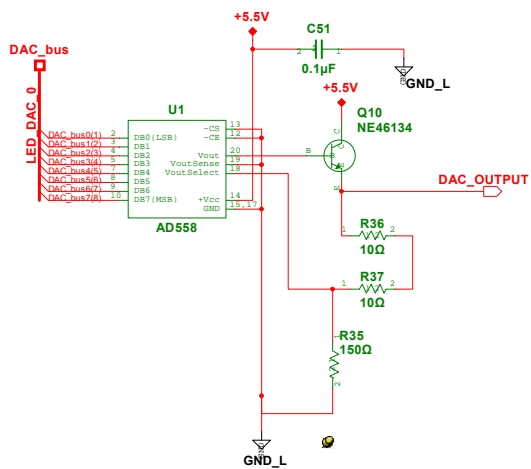
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 16 of 19




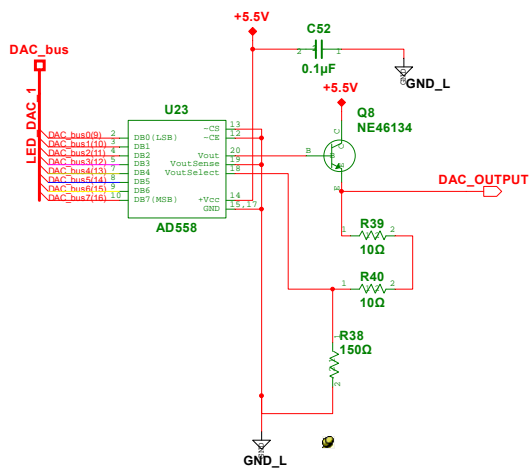
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Designer: © 2013,	Page Description: HE Pulser Rev2		
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Approved:	CAGE Code: 4B817	Date: 8/20/2015	Sheet: 19 of 19