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work on igloo2 DevKit (last entry on top)

14 Aug

Yesterday i found a max variation of the Rx Clk = (10.5 - 9.1) ns = 1.4 ns, correlated to RX_BITSLIP_NUMBER status register. This is in agreement with Jose's measurements [bottom of slide 10 of http://indico.cern.ch/event/284351/contribution/1/material/slides/1.pdf]
The interesting thing is that RX_BITSLIP_NUMBER of the FEE could be read from the Back-End Electronics (BEE), and the BEE could take action.
I want to see if i can get a smaller variation, observing RX_BITSLIP_NUMBER and forcing to re-establish the link (i'll do this by stopping and starting the communication via UART, without power cycles).
I set as a goal to obtain RX_BITSLIP_NUMBER > 15

NB: my HW setup is very touchy.

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	**Delay [ns]**	
7	9.75	
16	9.25	GOAL !

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	**Delay [ns]**	
19	9.05	GOAL !

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	**Delay [ns]**	
0	10.25	
1	10.2	
6	9.85	
19	9.1	GOAL !

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	**Delay [ns]**	
5	9.9	
11	9.55	
11	9.55	
0	10.25	
11	9.55	
16	9.2	GOAL !

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	Delay [ns]	
19	9.1	GOAL !

Power-cycle the two kits, then repeat :

RX_BITSLIP_NUMBER	Delay [ns]	
14	9.35	
4	10.0	
10	9.6	
8	9.75	
19	9.1	GOAL !

So, just looking at the RX_BITSLIP_NUMBER and resetting the link (operations that can be done from the Back End Electronics, automated by the sw), I have achieved the following delays of the Recovered Clock in the FEE: 9.25, 9.05, 9.1, 9.2, 9.1, 9.1 ns.
This corresponds to a max variation = (9.25 - 9.05) ns = 0.2 ns
The variation could be further reduced accepting a single value of RX_BITSLIP_NUMBER .

Now I make an approximate jitter measurement of the Recovered clock:
the recovered clock is sent to a heade pin as signle-end, use a single-end active probe
use the histogram function of the scope (horizontal hitogram placed on the middle of the rising edge of the signal).
Over 1 minute, the peak-to-peak variation is 150 ps. This probably has a large contribution from the hardware setup.
In order to make a better measure, i need to send out the Rec clock differentially. Assign as follow:
RX_FRAME_CLK → (C4, D5) → J1.43, J1.45
TX_FRAME_CLK → (F5, F6) → J1.37, J1.39

Measure the pk-pk jitter on Kit SN 8 RX_FRAME_CLK → (C4, D5) → J1.43, J1.45 with a differential probe; it is 300 ps.
It is strange tha t it is bigger than with single-end signal and probe.

13 Aug

Prepare the two Dev kits SN 7 and SN 8, test fw LATOP\GBT_On_Igloo2_M2GL_EVAL_KIT_LATOP.stp (SVN Rev 4718) transmitting from SN 7 to SN 8.

Each kit has the following signals available on pins on connector J1:

TX_WORD_CLK → AB15 → J1.1 expected ~240 MHz (an igloo2 20-bit SERDES word)
TX_FRAME_CLK → AA15 → J1.3 expected ~40 MHz (a GBT 120-bit frame)
RX_WORD_CLK → AA16 → J1.6
RX_FRAME_CLK → AB18 → J1.7
TX_MATCH_FLAG → AA17 → J1.8
RX_MATCH_FLAG → AB19 → J1.9
RX_HEADER_FLAG → AB17 → J1.12

With the scope TDS7254, i probe SN 7 TX_FRAME_CLK and SN 8 RX_FRAME_CLK.
The two clocks are in sync (good, link is established, as confirmed by the UART interface).
This is a measurement of the phase stability of the recovered clock
I trigger the scope on SN 7 TX_FRAME_CLK; i choose a clear crossing point for the two signals, and use the vertical cursors of the scope..
I take this measurements, power cycling both kits before each measure:

Delay [ns]	**RX_BITSLIP_NUMBER via UART**
9.1	19
9.7	10
10	6
9.35	14
10.5	1
10.5	1
9.55	12
9.5	13
10.05	6
9.85	9

Now leave the system running after the last measure (9.85 ns ; bitslip = 9) at time h15:13.
I want to measure the stability leaving the system running without power cycles.
At time 15:22 still the same.
At 15:31 still the same. Stop the system.