HF QIE Prototype Board Review

U79 - PROASIC FPGA

Everything seems fine, except for some typos in the schematics.

Power Supplies and Grounds

Ground (GND, GNDQ)

- ✓ All GND grounded.
- ✓ All PLLs (VCOMPLA/B/C/D/E/F) grounded.
- ✓ All PLLs (VCCPLA/B/C/D/E/F) grounded.

VCC (Supply voltage for the core = 1.5 V)

- ✓ All VCC pins checked, ok.

VCCIBx (Supply voltage to the output buffer of each bank x = 0 to 7)

- ✓ All VCCIB0-VCCIB6 connected to 2.5 V
- ✓ All VCCIB7 connected to 3.3 V

VMVx (Quiet supply voltage to the input buffer of each bank x = 0 to 7)

- ✓ All VMV0-VMV7 connected to 2.5 V

VJTAG

- ✓ Connected to 2.5 V

VPUMP

- ✓ Connected to 2.5 V

Signals

JTAG

- ✓ TRST, TDI, TCK, TDO and TMS connected to J6.

Some typos where found on the schematic:

QIE_8

- ✓ **W25 Qie8_Out_N[3]**
  schematic -> IO136NDB3V2, Datasheet -> IO136NPB3V2.

QIE_4

- ✓ **E17 Qie4_DiscOut_P**
  schematic -> IO49PDB1V0, Datasheet -> IO49PDB1V1.
- ✓ **E16 Qie4_DiscOut_N**
  schematic -> IO49NDB1V0 Datasheet -> IO49NDB1V1.

QIE_5

- ✓ **C17 Qie5_Out_P[4]**
  schematic -> IO55PDB1V1, Datasheet -> IO55PPB1V1.
- ✓ **D18 Qie5_Out_P[4]**
  schematic -> IO55NDB1V1, Datasheet -> IO55NPB1V1.

QIE_6

- ✓ **H22 Qie6_Rst_P**
  schematic -> IO70PPB1V3, Datasheet -> IO70PDB1V3.
- ✓ **H21 Qie6_Rst_N**
  schematic -> IO70NPB1V3, Datasheet -> IO70NDB1V3.

U81 - Bridge PROASIC FPGA

Bridge FPGA. Pins mismatched:

pin	--	from PDC	---	from PCB/Altium
E8	--	MClk_P	---	BKLPLN_SPARE3
F8	--	MClk_N	---	BKLPLN_SPARE1
F11	--	BRD_PWR_GOOD_25	---	BKLPLN_SPARE4
G8	--	BkPln_RES_QIE	---	BRD_PWR_GOOD_2.5
G11	--	BKLPLN_SPARE[1]	---	CLK_Bridge_40MHz_N
G12	--	BKLPLN_SPARE[3]	---	CLK_Bridge_40MHz_P
J4	--	BkPln_WTE	---	UniqueID_SDA
K1	--	BkPln_RES	---	UniqueID_SCL
K9	--	UniqueID_SCL	---	EMPTY
M4	--	UniqueID_SDA	---	EMPTY

U80 - IGLOO2 FPGA

There was no pinout reference for this FPGA, so we just checked the consistency between the schematics and the PCB.

There are two swapped connections:

pin	--	from Schematic	---	from PCB/Altium
G2	--	BK_RES	---	BK_WTE
G3	--	BK_WTE	---	BK_RES

J1, J5

J1 - The sequence Ref, Signal is inverted just for channel 12.
J5 - The sequence Ref, Signal is inverted just for channel 24.