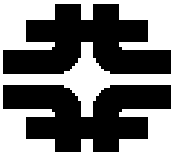

Fermilab

Particle Physics/Electrical Engineering Department

The CMS Hadron Calorimeter
HF 24 Channel Front-End Prototype Module

Revised
11/2/2013

Revision History

Introduction

The 24-Channel HF Front-end Prototype module is being produced to test the design concept(s) for the pre-production and production modules. The block diagram for the module is shown in Figure 1.

Figure 1 shows that 24 QIE10 ASICs[1] will be used to read out 24 PMT analog input signals. The PMT signals are transmitted as a signal and return pair over 5 meter of 50 ohm multi-coax cables. The cable and its board mount connector were custom purchases[2]. Each 5 meter cable contains 24 individual coax cables which allow us to transmit signal/return from 12 PMTs. Two front panel connectors on each board handle 24 PMT signal.

The PMT signals are digitized by the QIEs, the digital data is then processed and sent off board via fiber optic links.

Design Considerations

Due to scheduled availability of components and the desire to test two possible design concepts, the board is being designed to handle the data flow from the QIEs in two different methods. Twelve QIEs (1-12), see Figure 2, will be read out using the design described in the Technical Design Report[3]. Thus; twelve QIEs will send data to a ProASIC FPGA which will receive the data, process it and transmit it to three GBTX ASICs[4]. The GBTX will use the VTTX[5] electrical/optical transmitters to send the data off board.

The other 12 QIE (13-24) channels, see Figure 3, will send the data to a newly developed Igloo2[6] FPGA which will be tested on this board. This FPGA has the advantage that it has a built in serializer which will work in a radiation environment. Thus, the GBTX is not required as a serializer and the data stream can be sent directly to the VTTX.

The GBTX serves as not only a serializer, but also provides multiple copies of low jitter independently phased clocks. In the event the GBTX is not available for this board (or the production modules), a commercial clock cleaner is being designed and will be tested on this board. QIE channels 13-24 will allow for a selection of clock signals which will come from this commercial clocking solution or from one of the GBTX ASICs onboard.

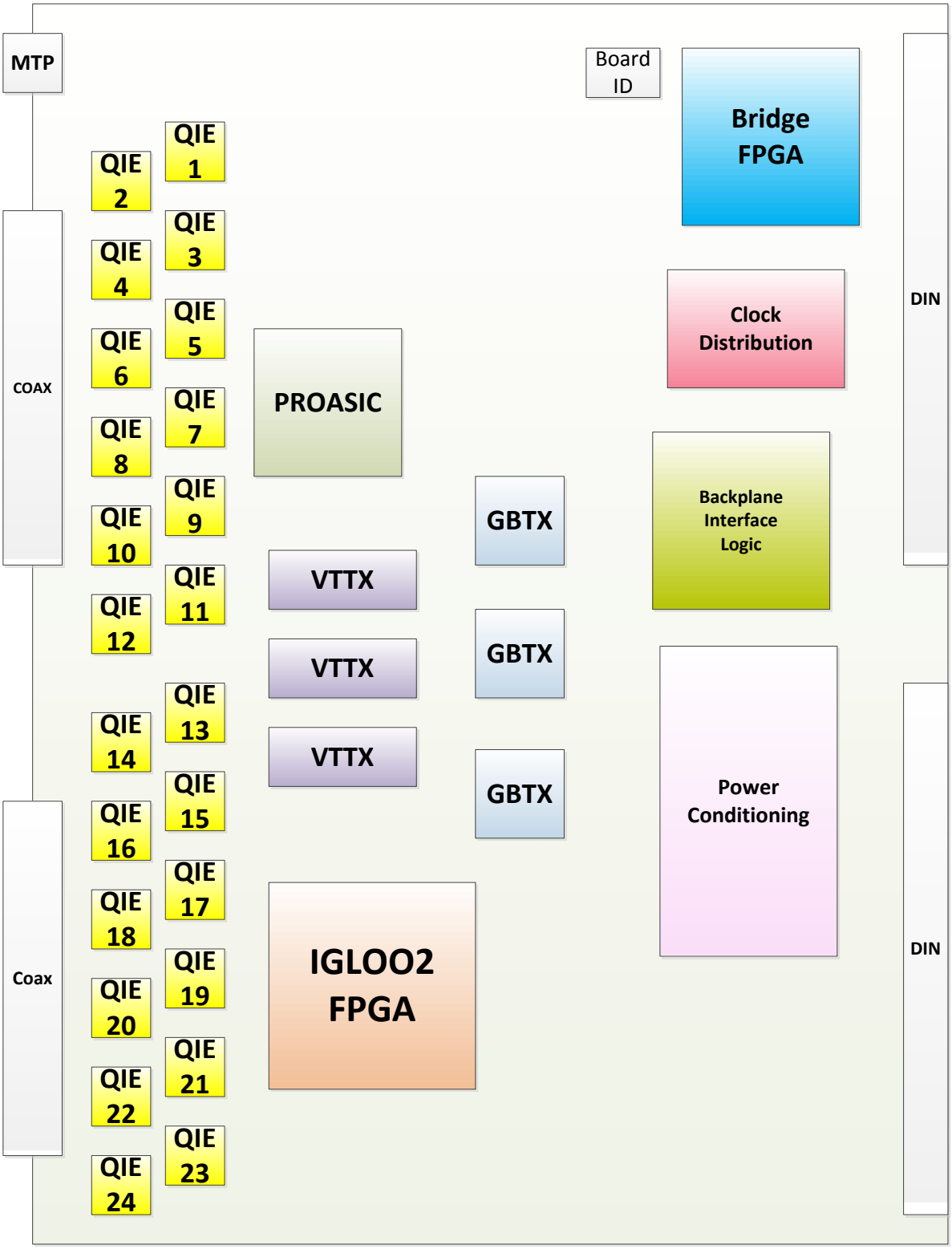

Figure 1. Block Diagram of HF 24-Channel Prototype Design Elements

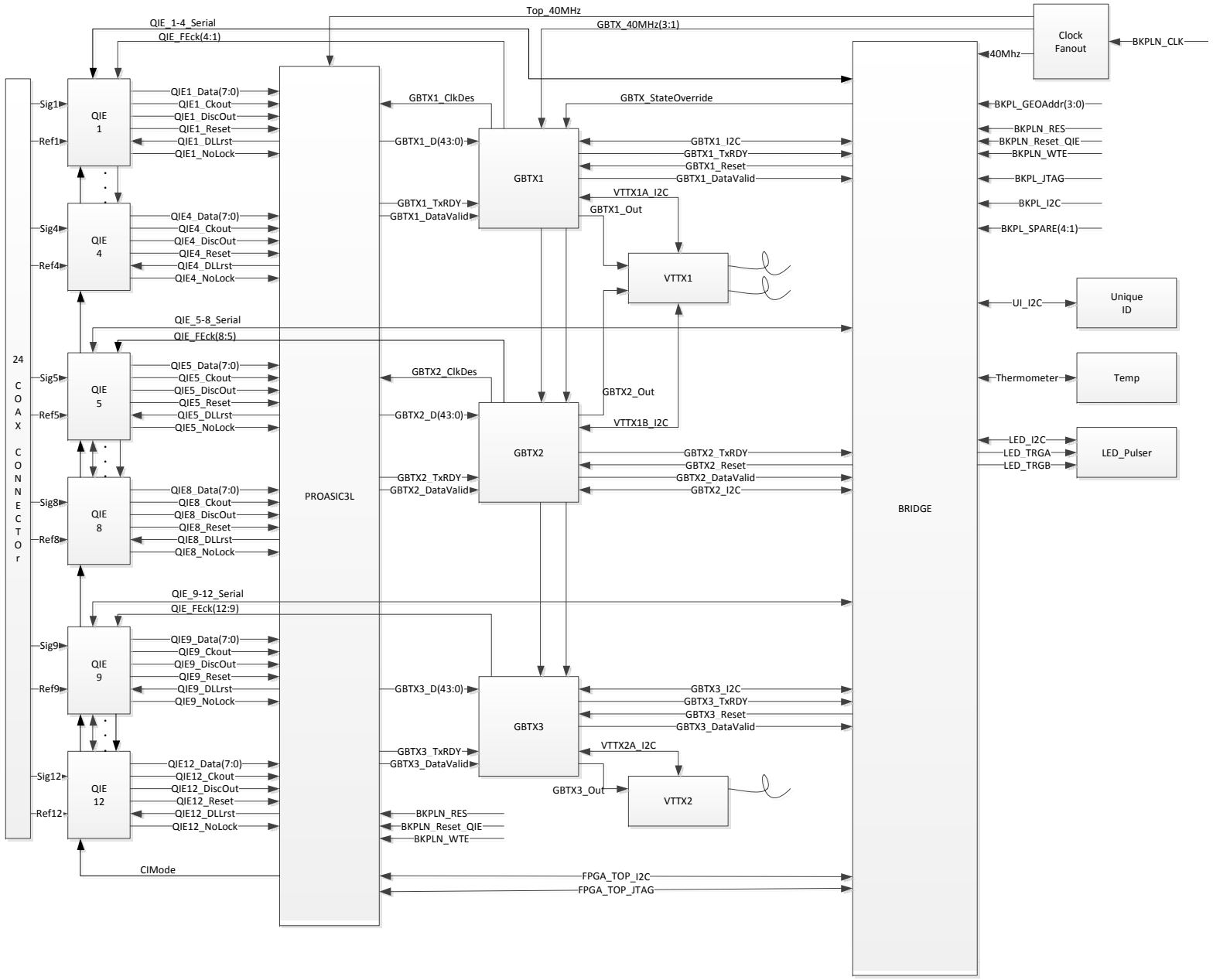

Figure 2. Block Diagram of QIE 1 through 12 Data Flow and Control

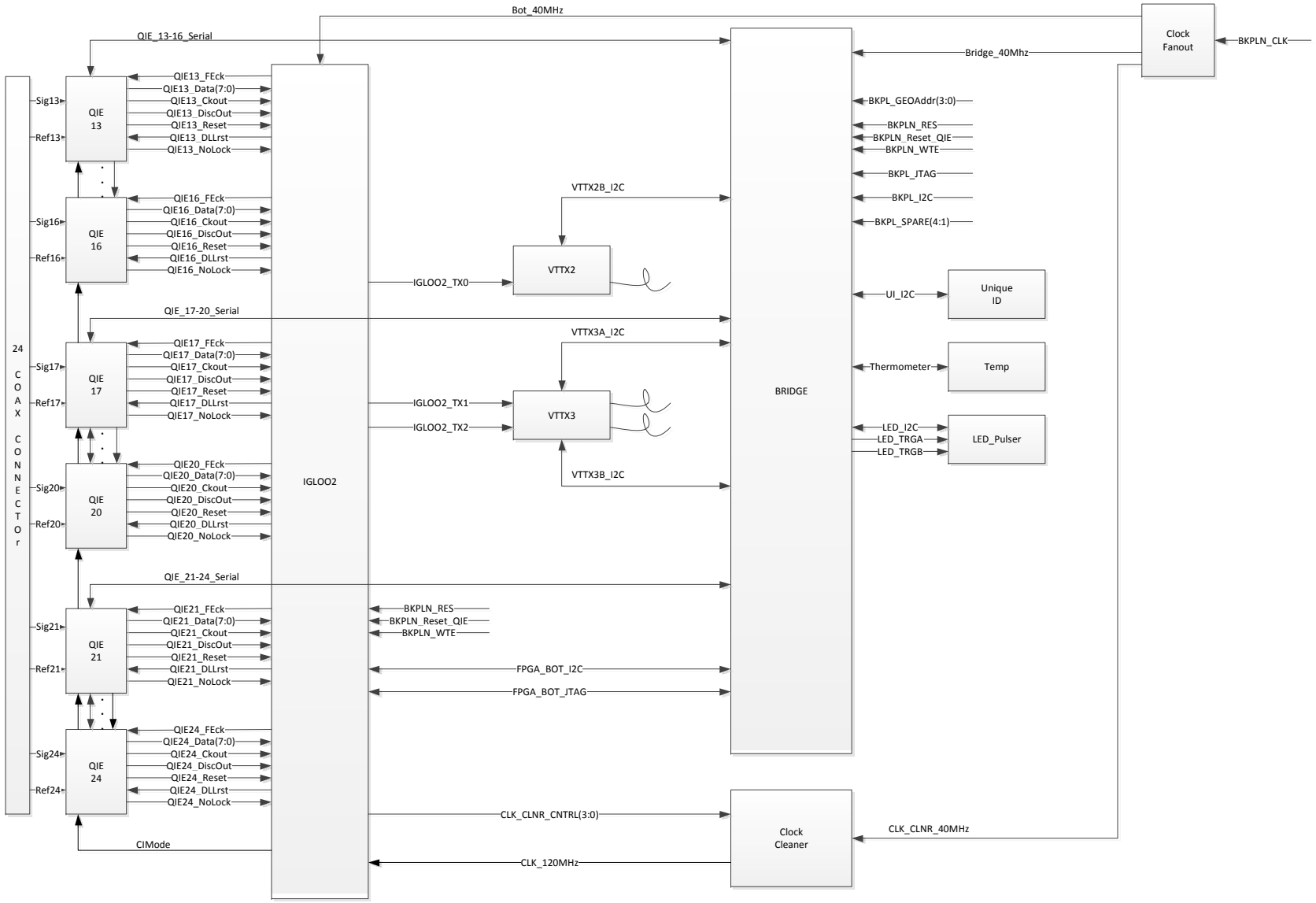

Figure 3. Block Diagram of QIE13 through QIE 24 Data Flow and Control

Power Section

To be added.

Refereneces:
(have to update)
[1] QIE Specification
[2] Winchester Cable Documentation
[3] TDR
[4] GBTX
[5] VTTX Specification
[6] ProASIC specification
[7] DC/DC Converter specification